

FIG. 1

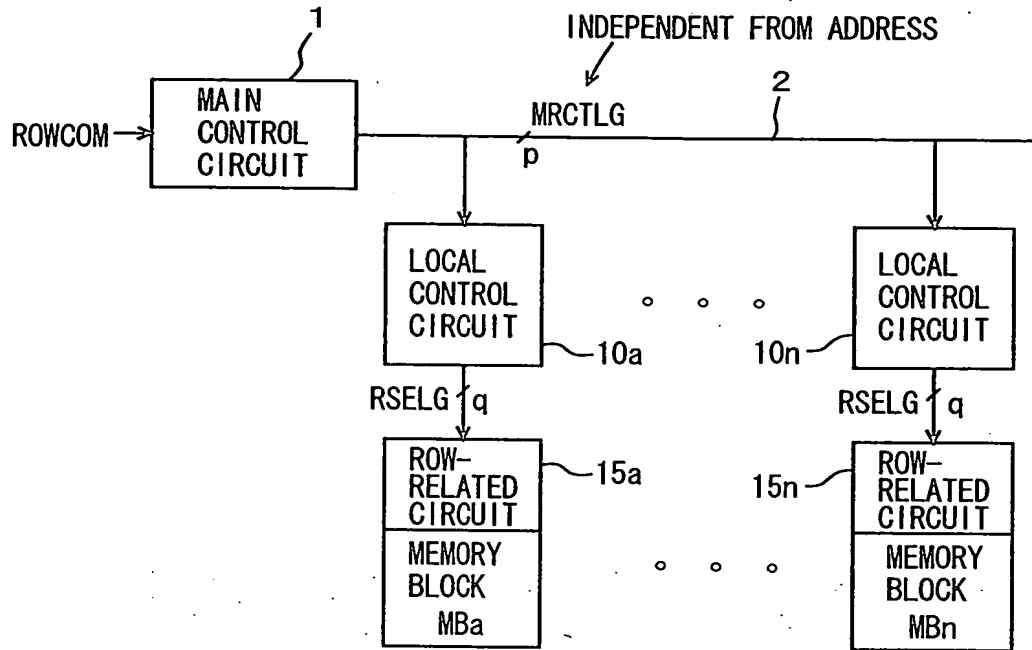
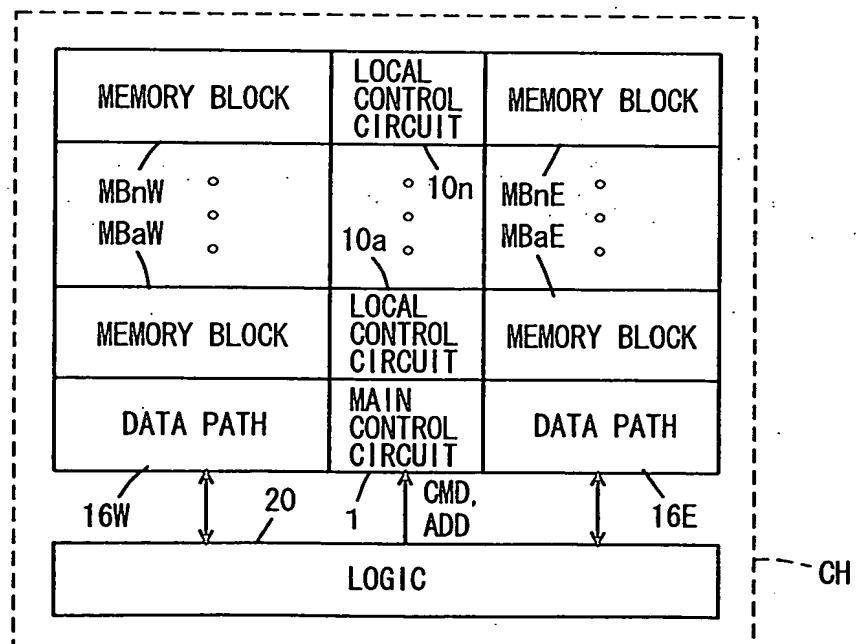


FIG. 2



• •

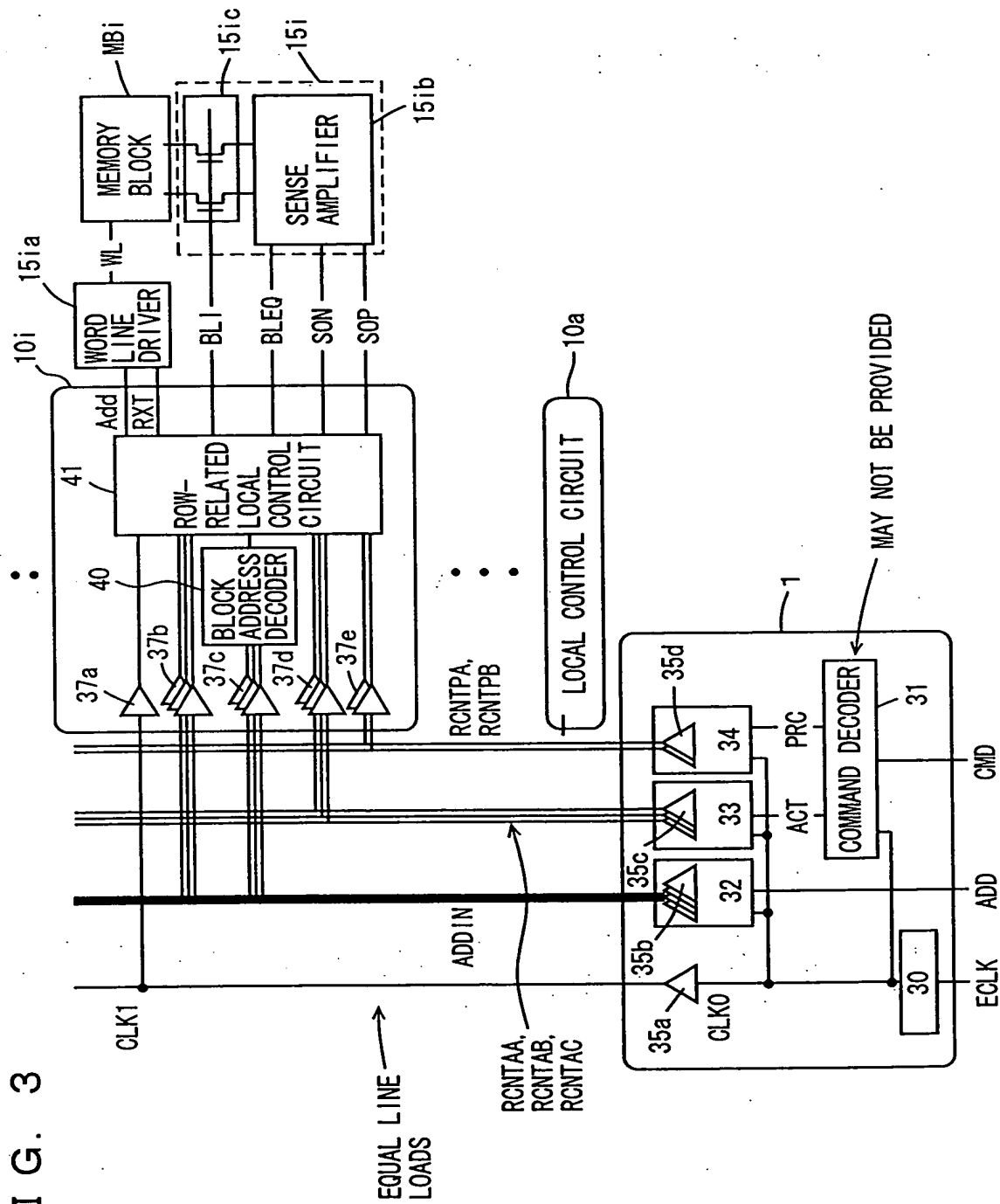
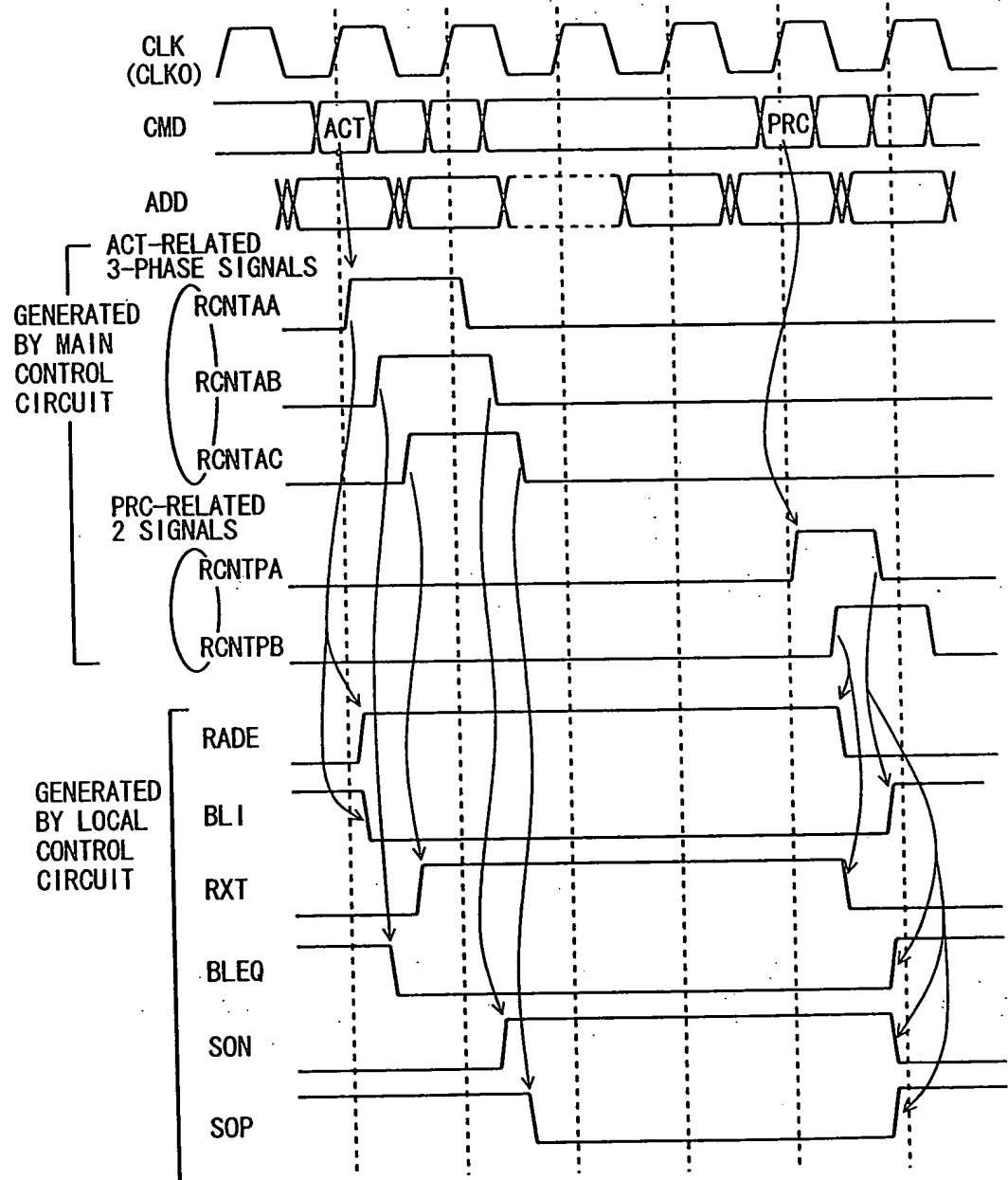


FIG. 4



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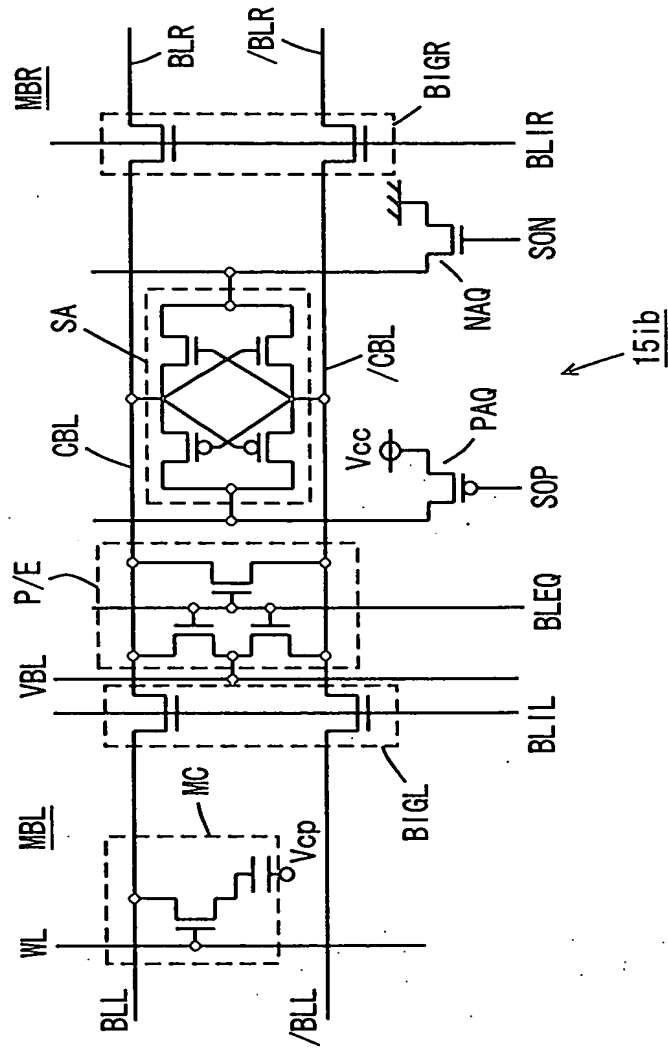


FIG. 6

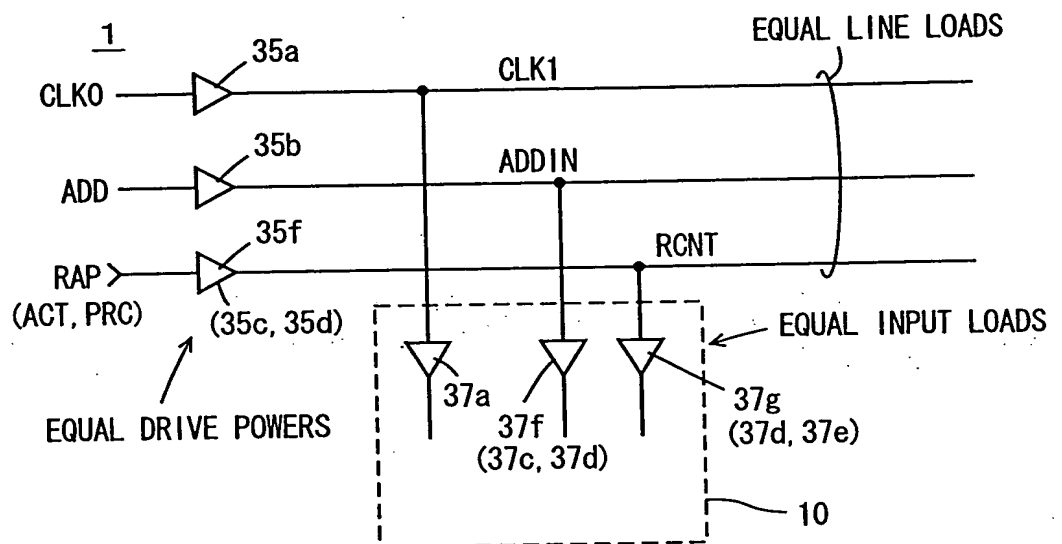


FIG. 7

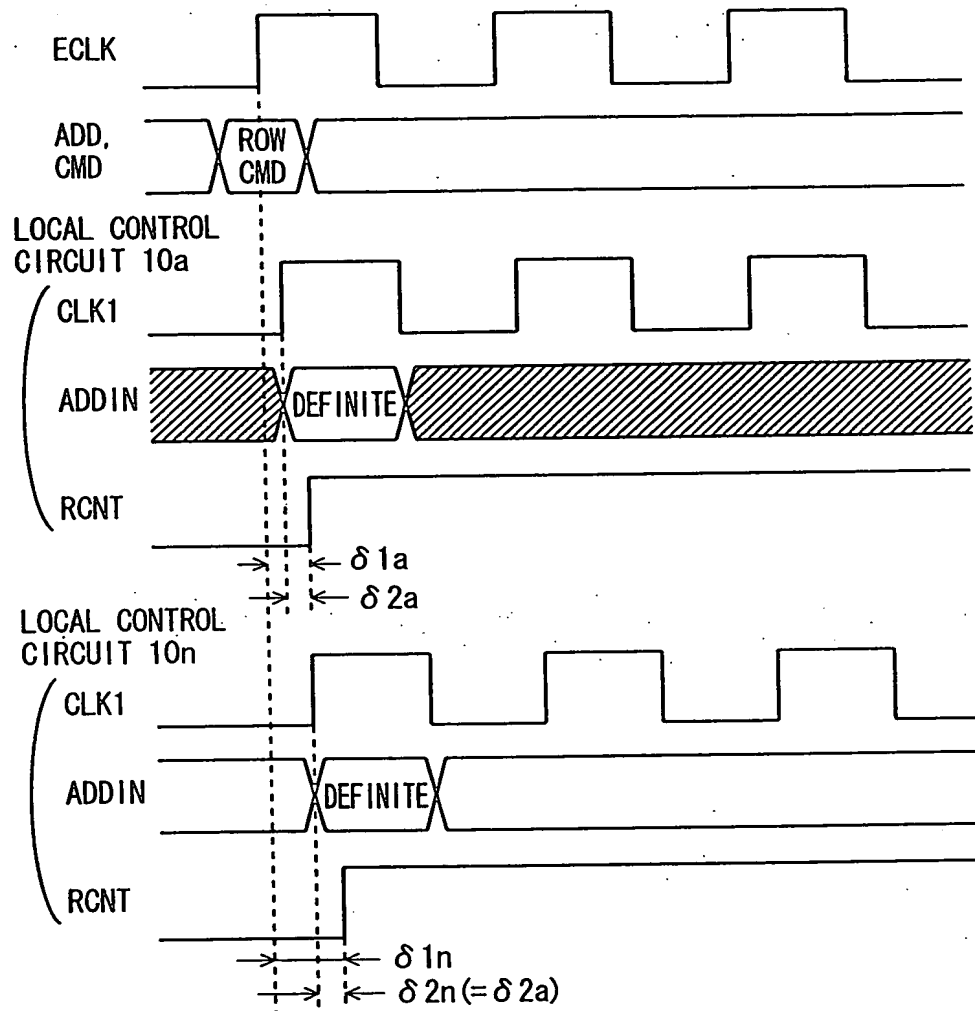


FIG. 8

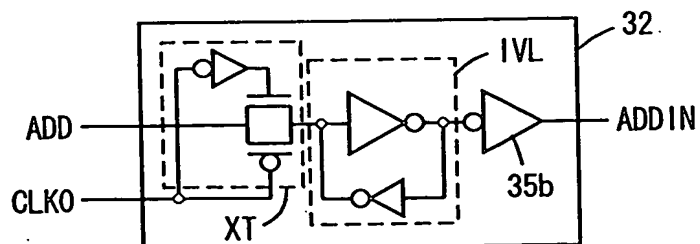


FIG. 9A

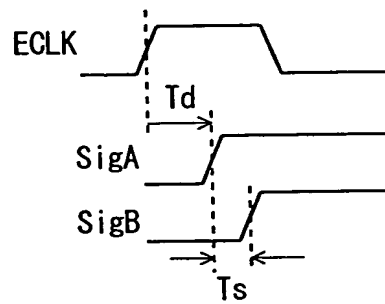


FIG. 9B PRIOR ART

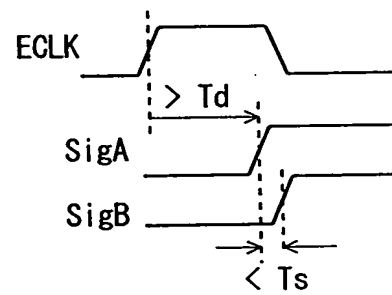


FIG. 9C

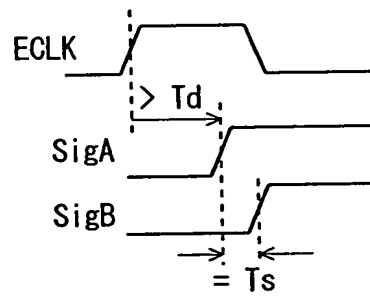


FIG. 10A

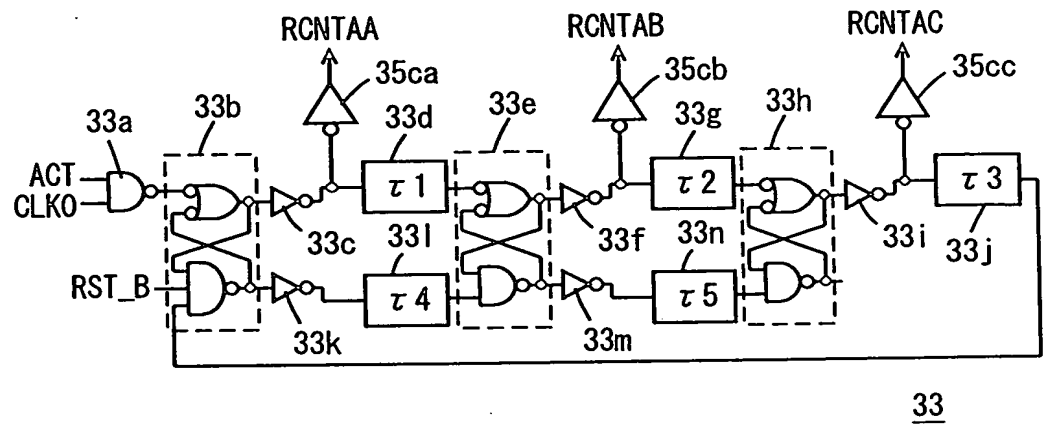


FIG. 10B

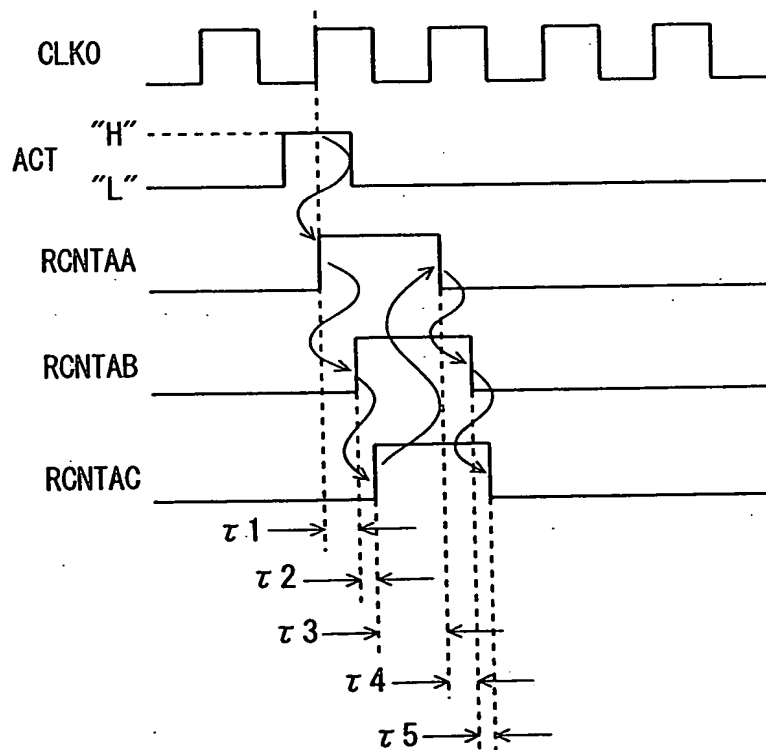


FIG. 11A

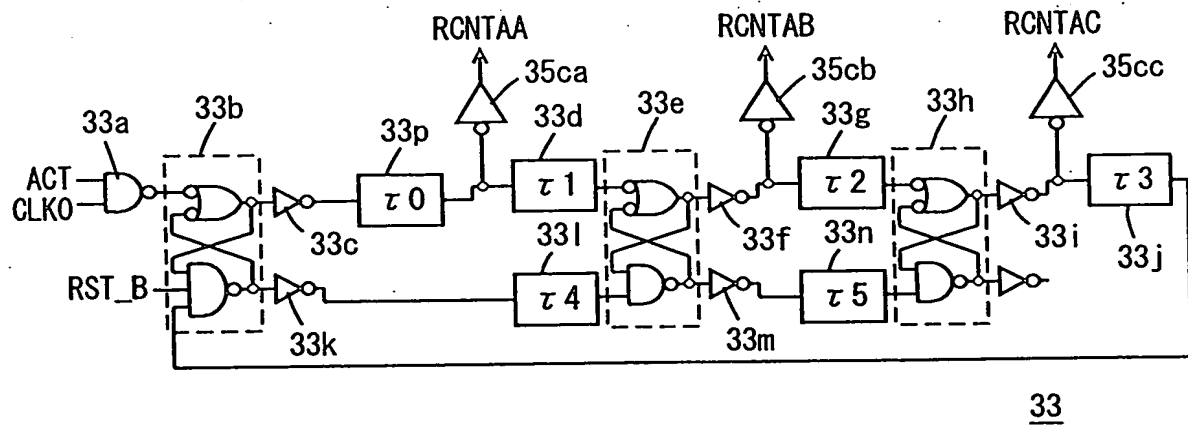


FIG. 11B

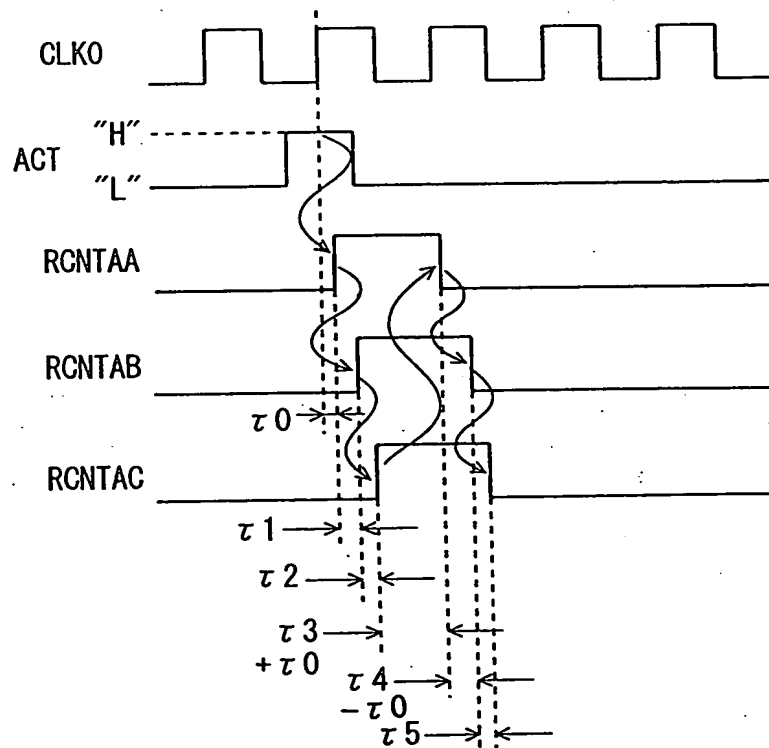


FIG. 12A

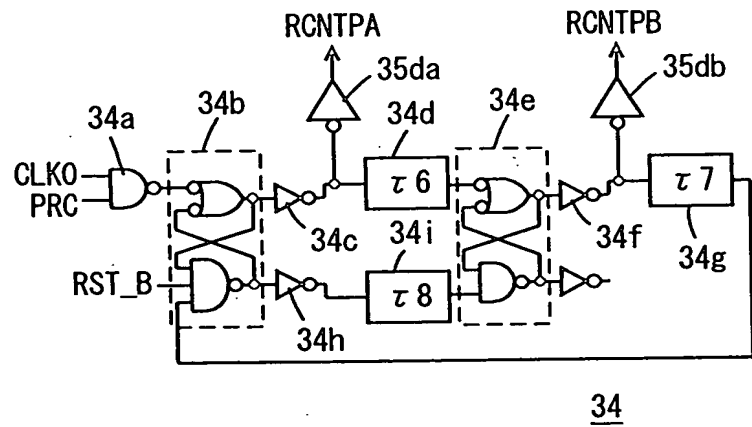


FIG. 12B

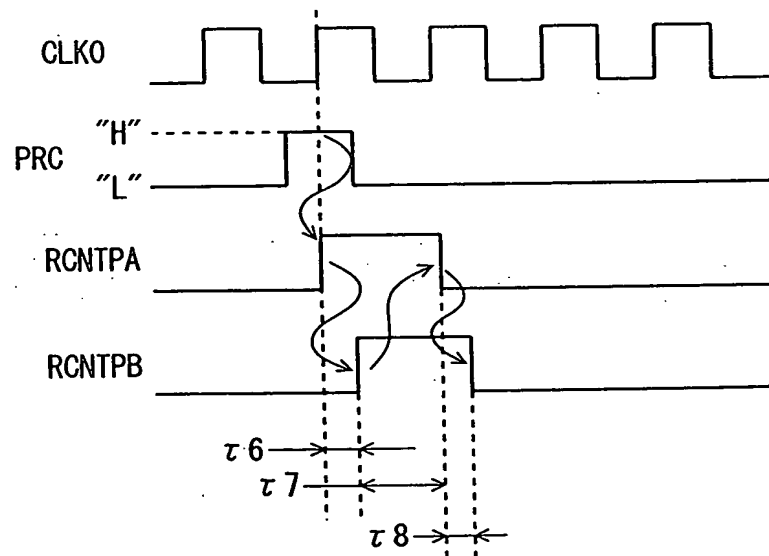


FIG. 13A

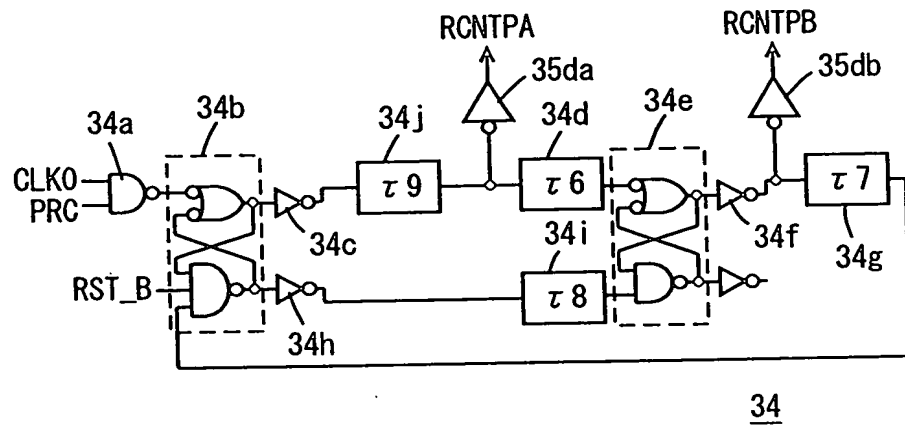


FIG. 13B

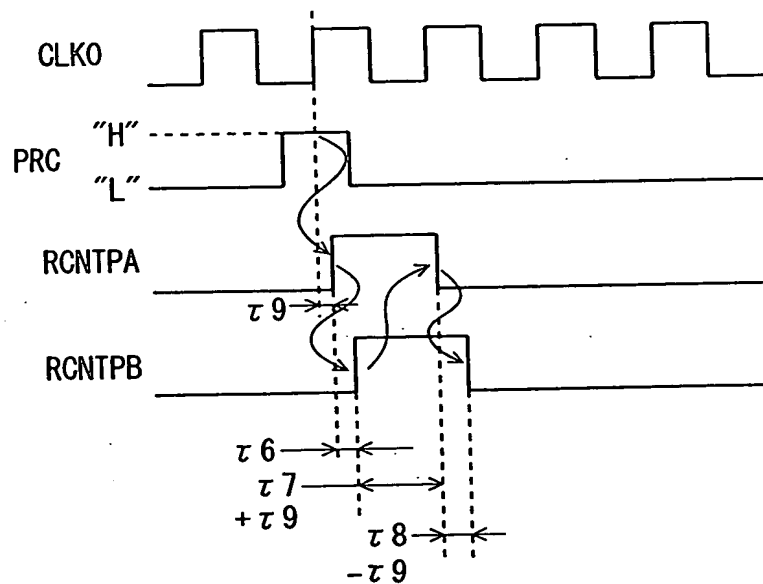


FIG. 14

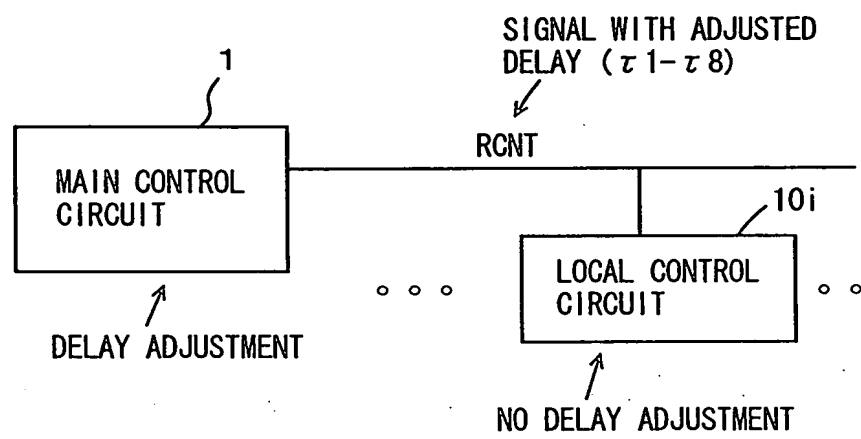


FIG. 15A

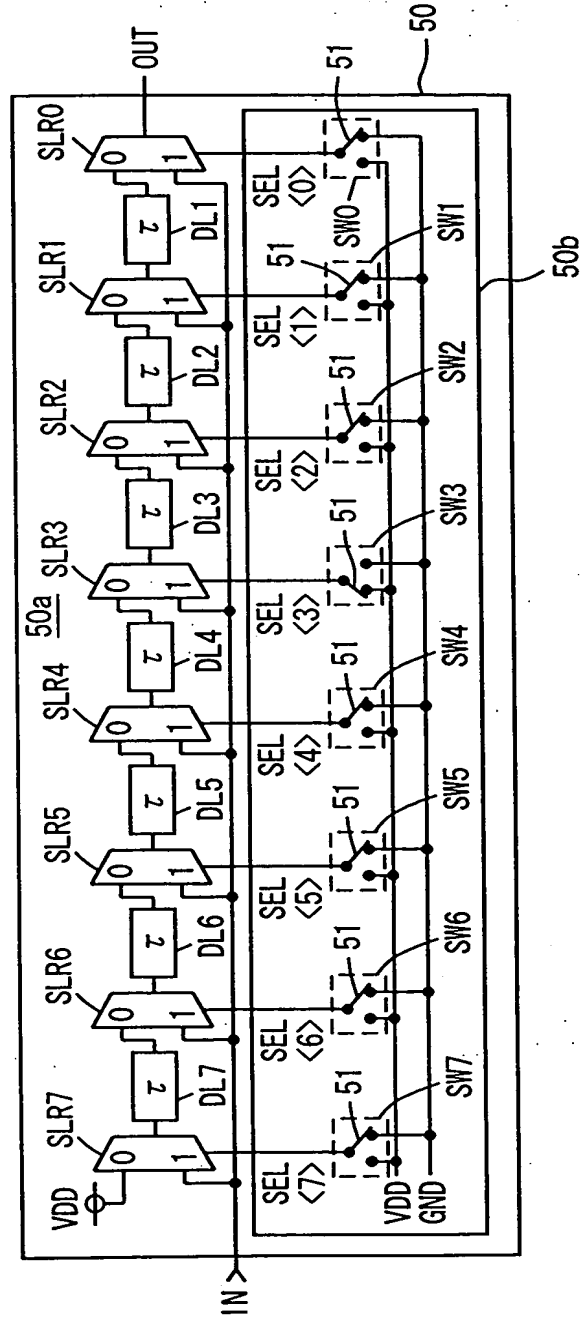


FIG. 15B

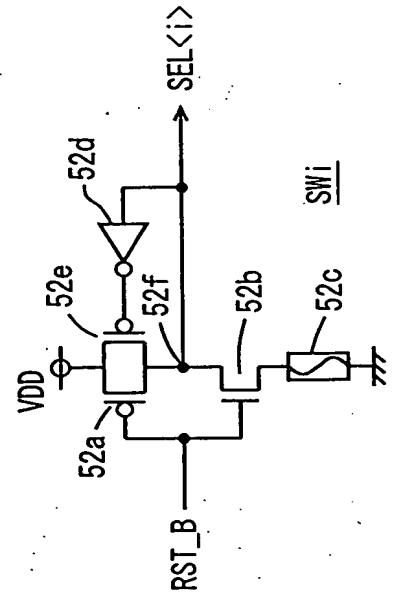


FIG. 16

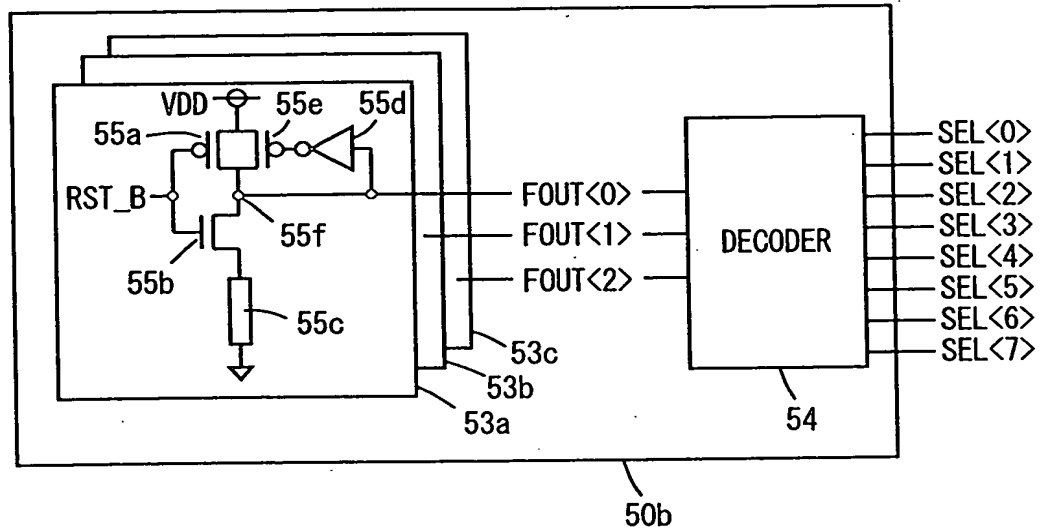


FIG. 17

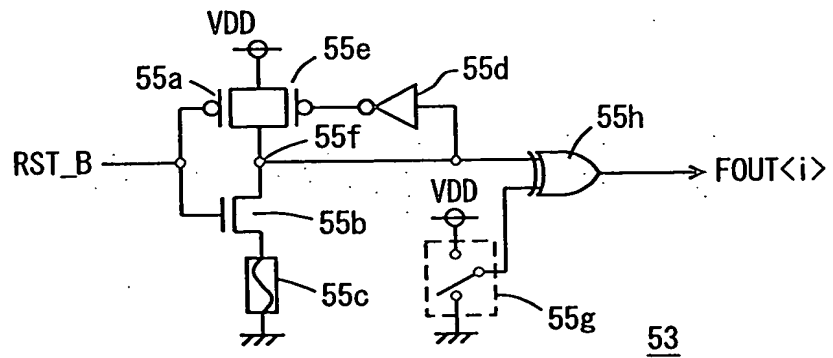


FIG. 18

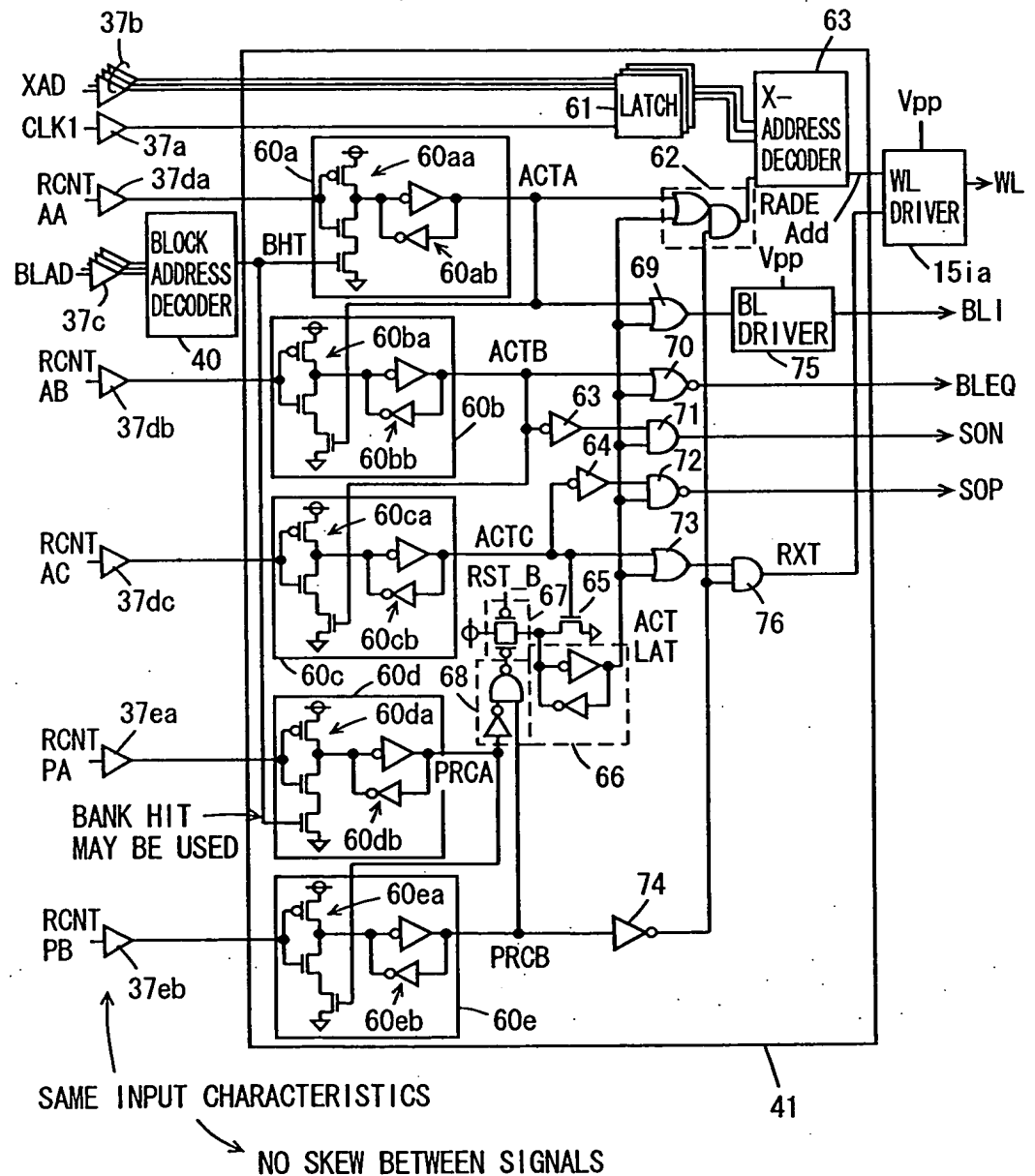


FIG. 19

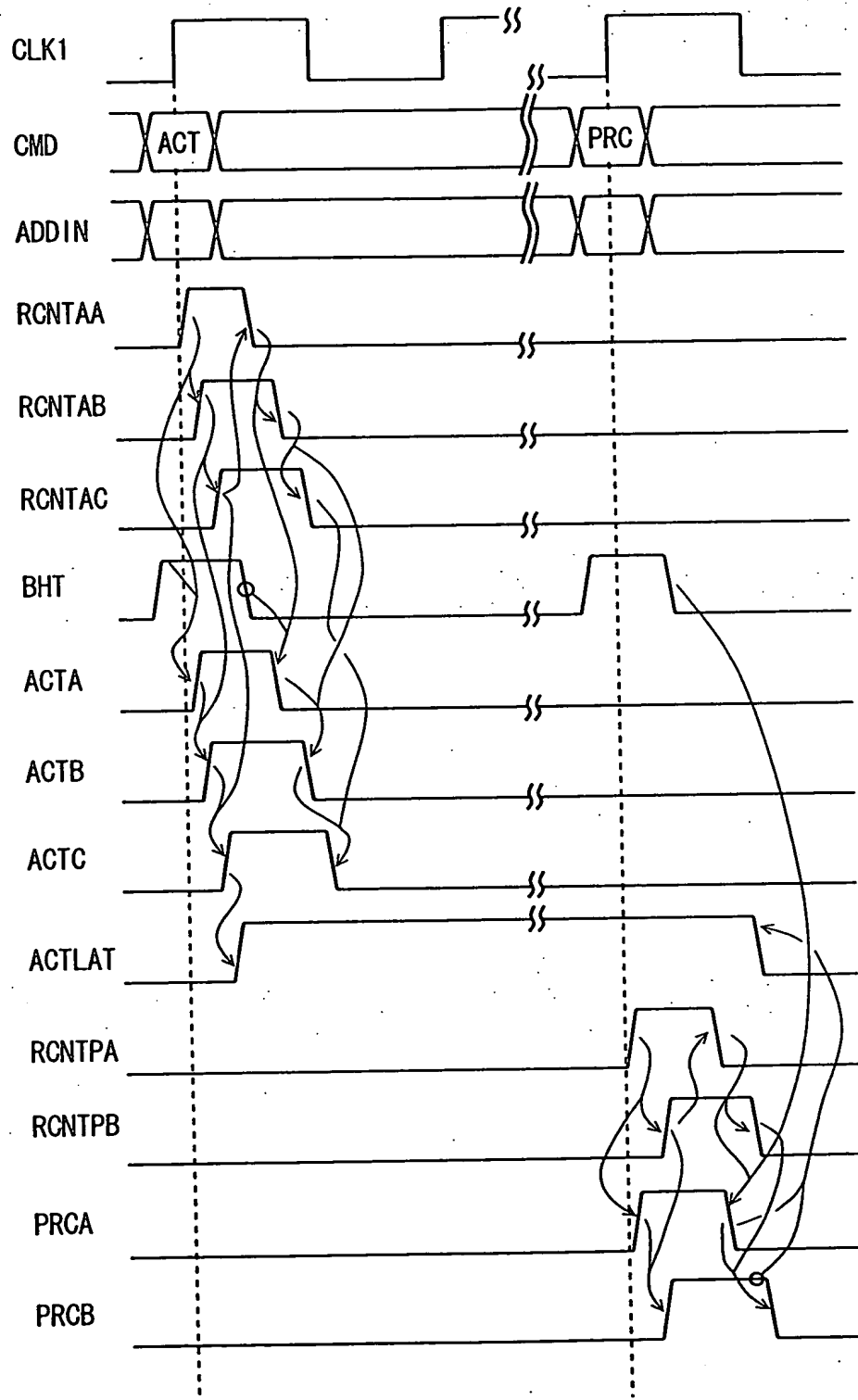


FIG. 20

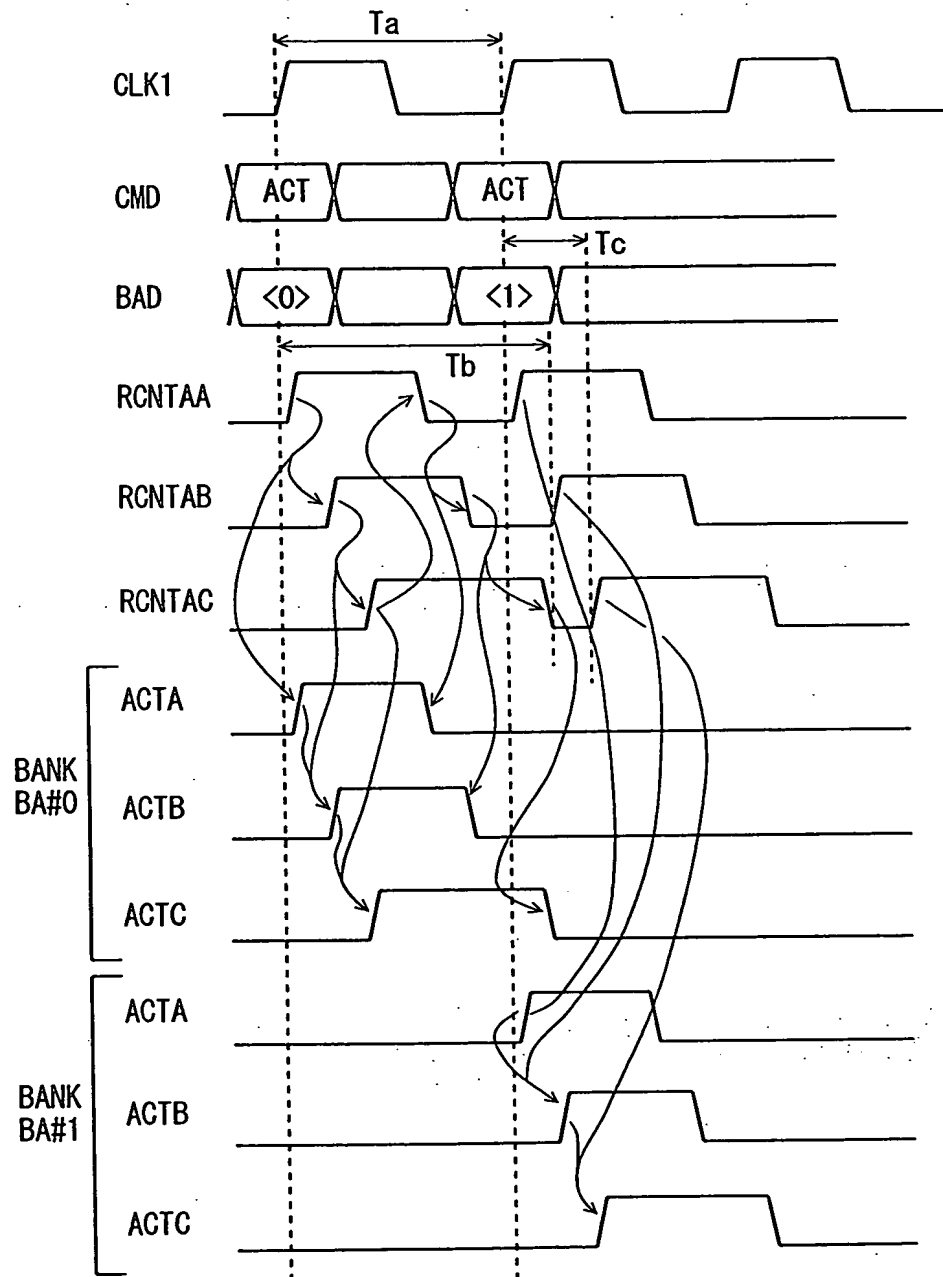


FIG. 21

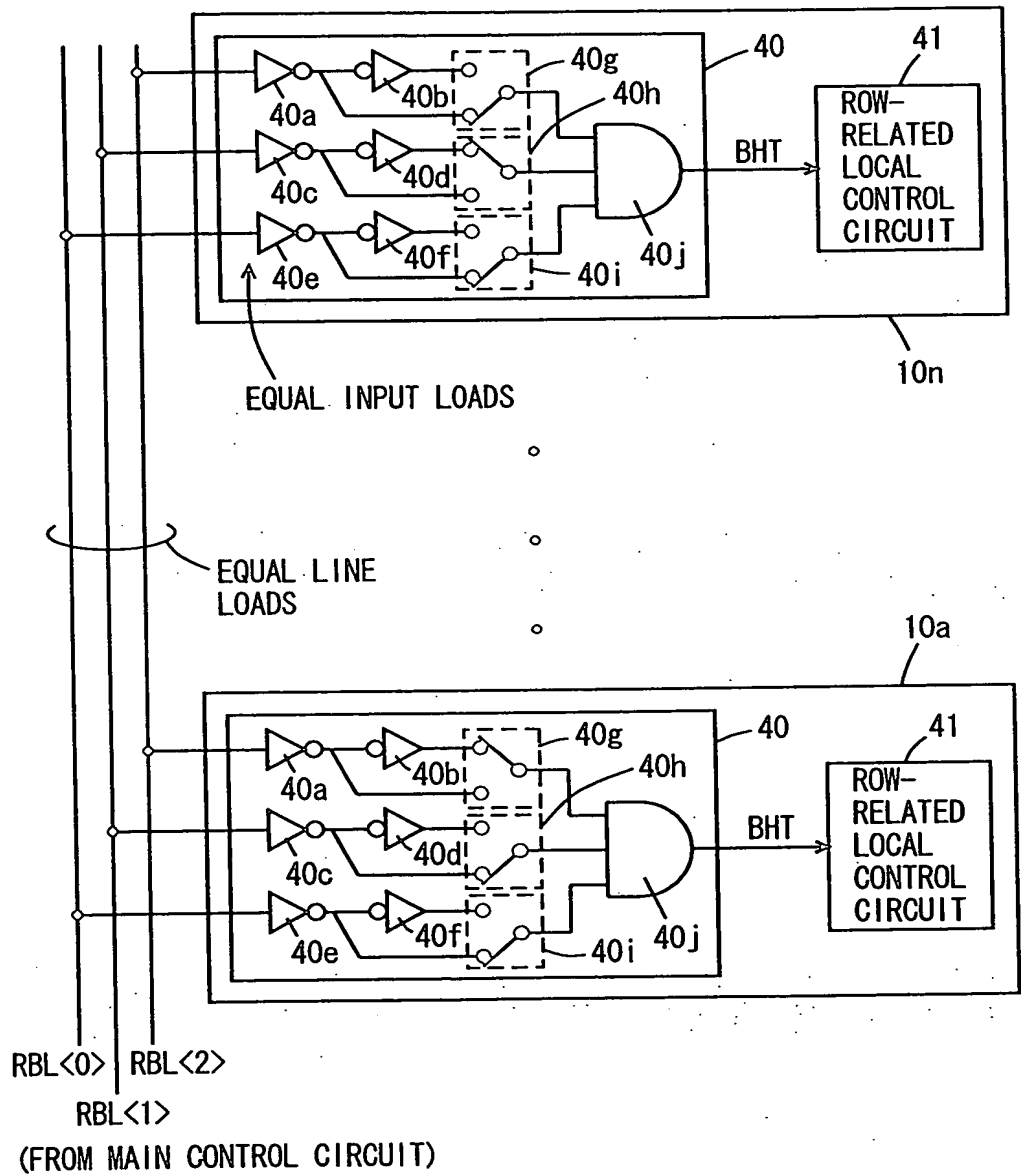


FIG. 22

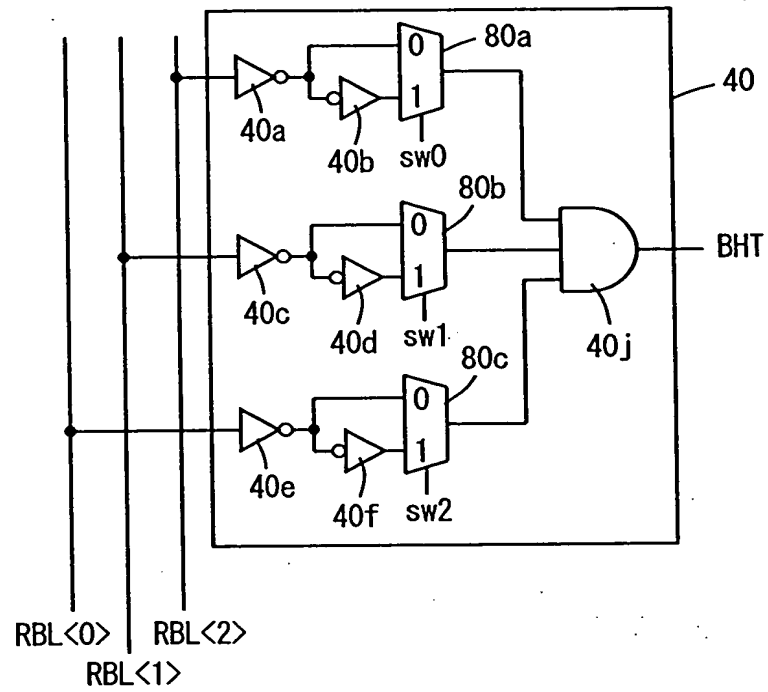


FIG. 23

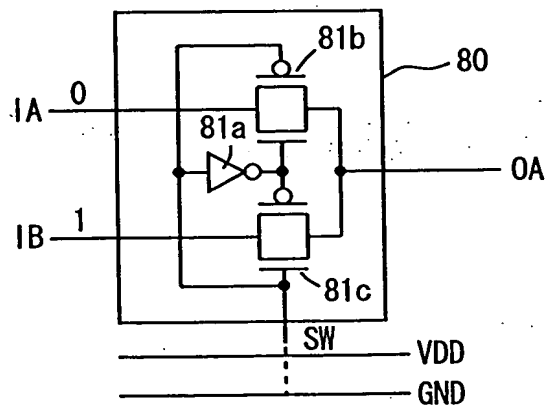


FIG. 24

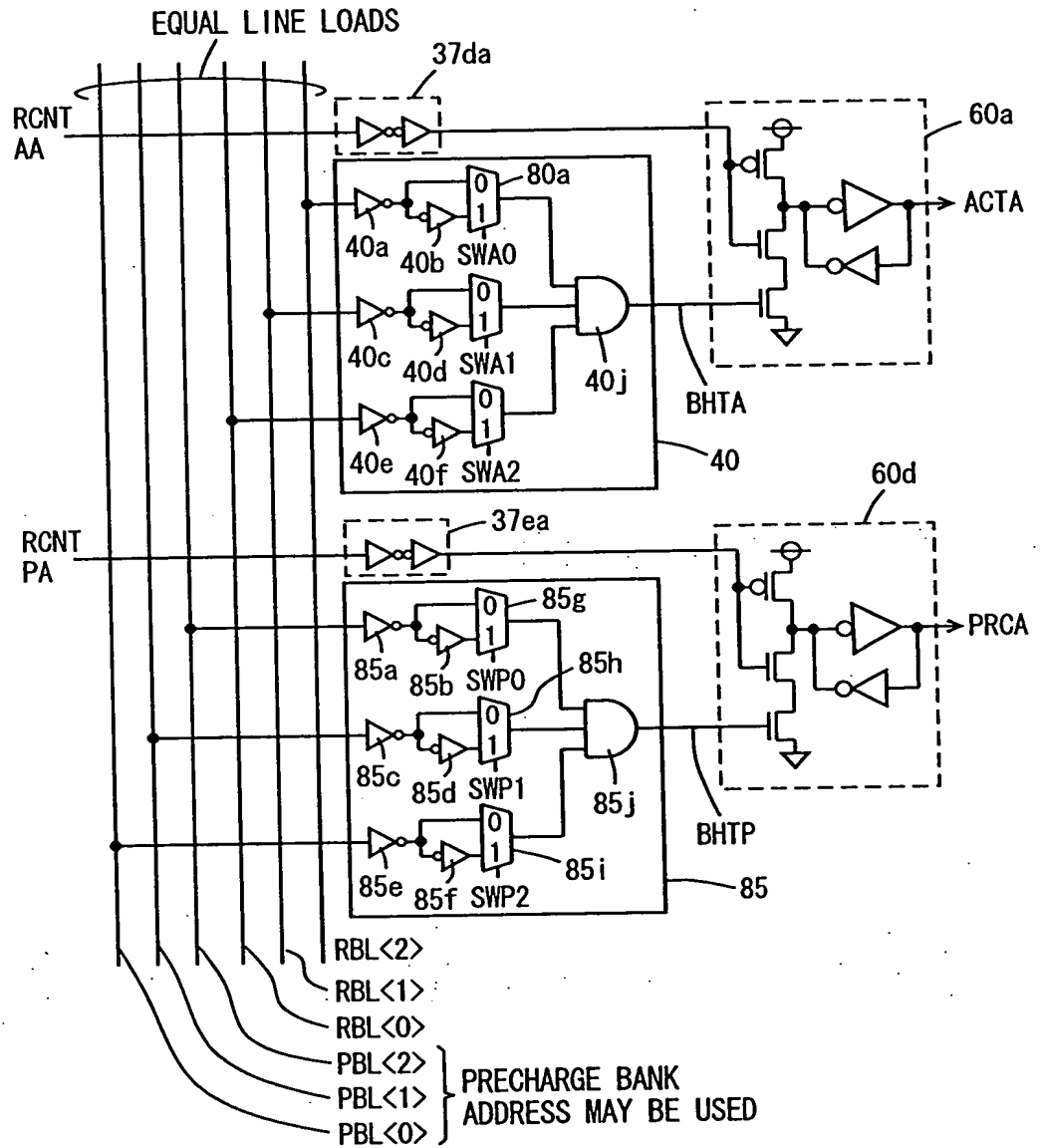
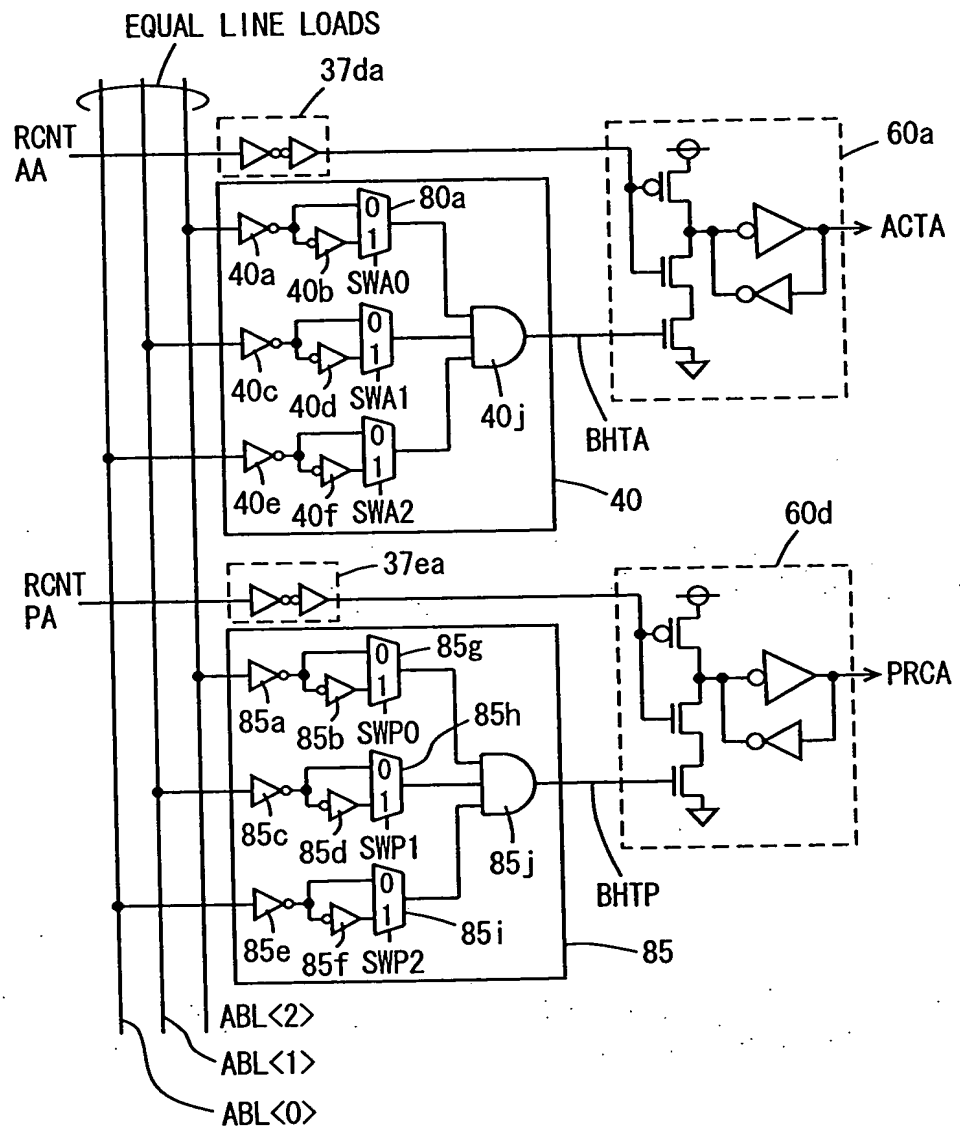


FIG. 25



: WHEN PRECHARGE IS PERFORMED A BANK
(A PLURALITY OF MEMORY BLOCKS) AT A TIME,
PRECHARGE BANK ADDRESS BITS ARE USED

FIG. 26

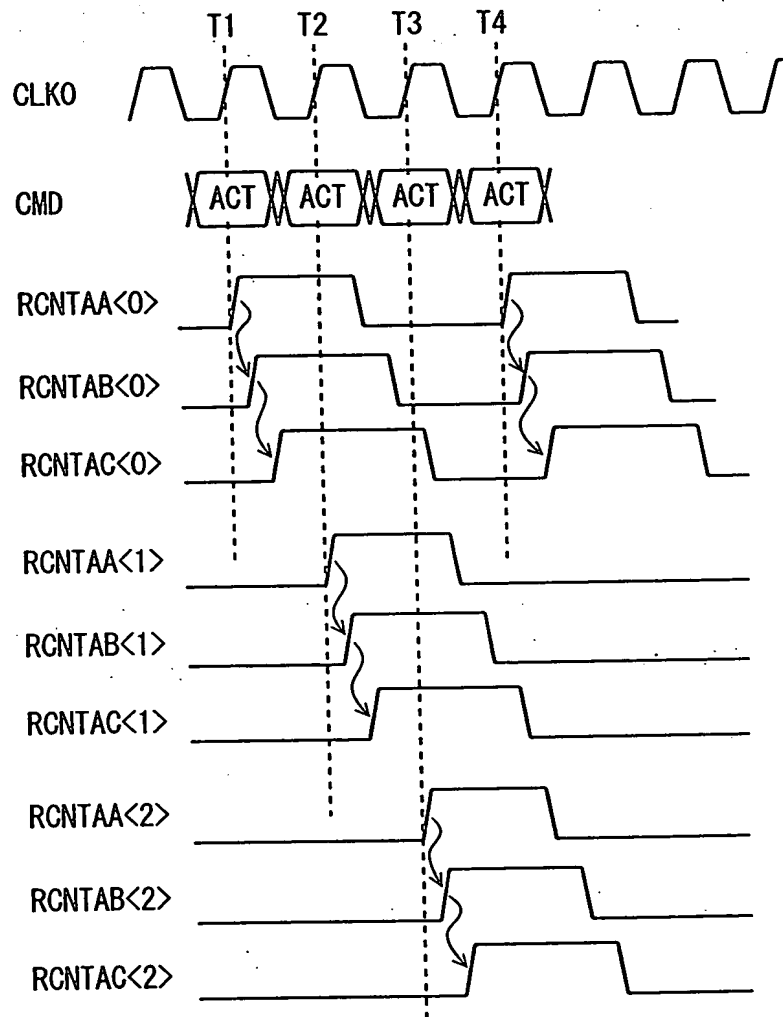


FIG. 27

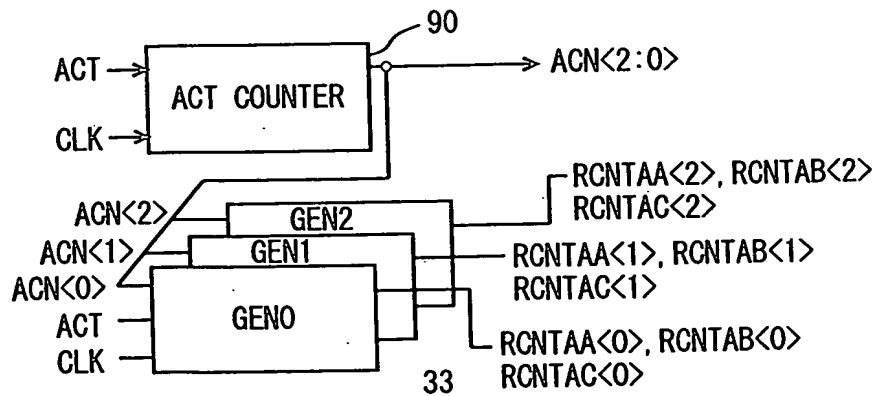


FIG. 29

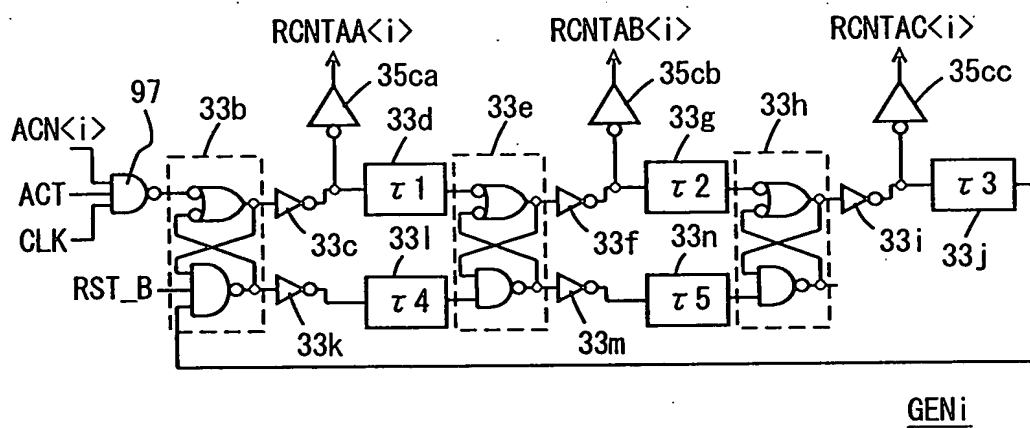


FIG. 30

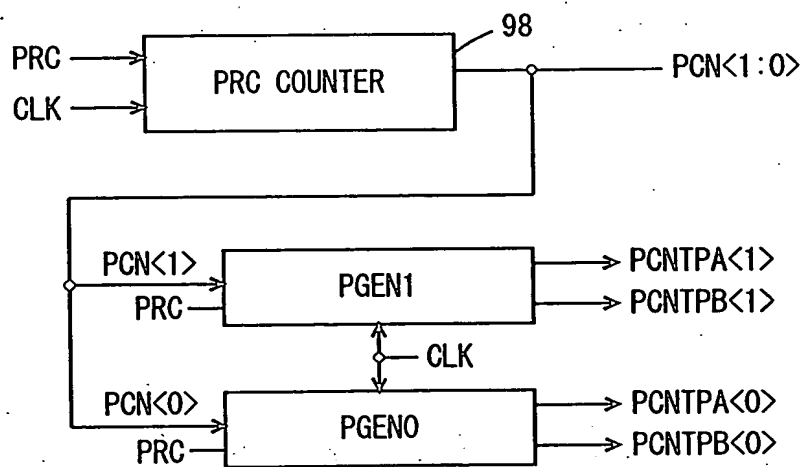


FIG. 31

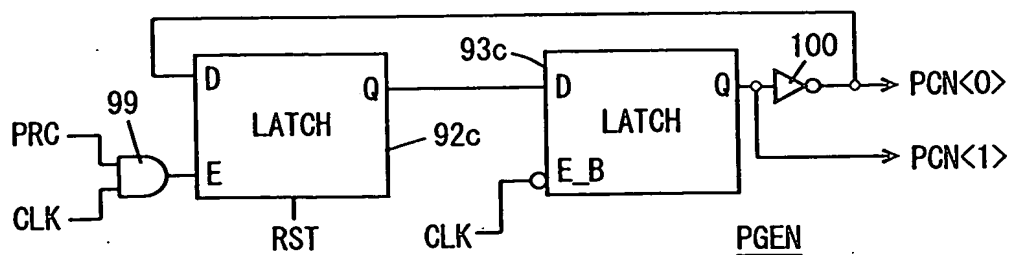


FIG. 32

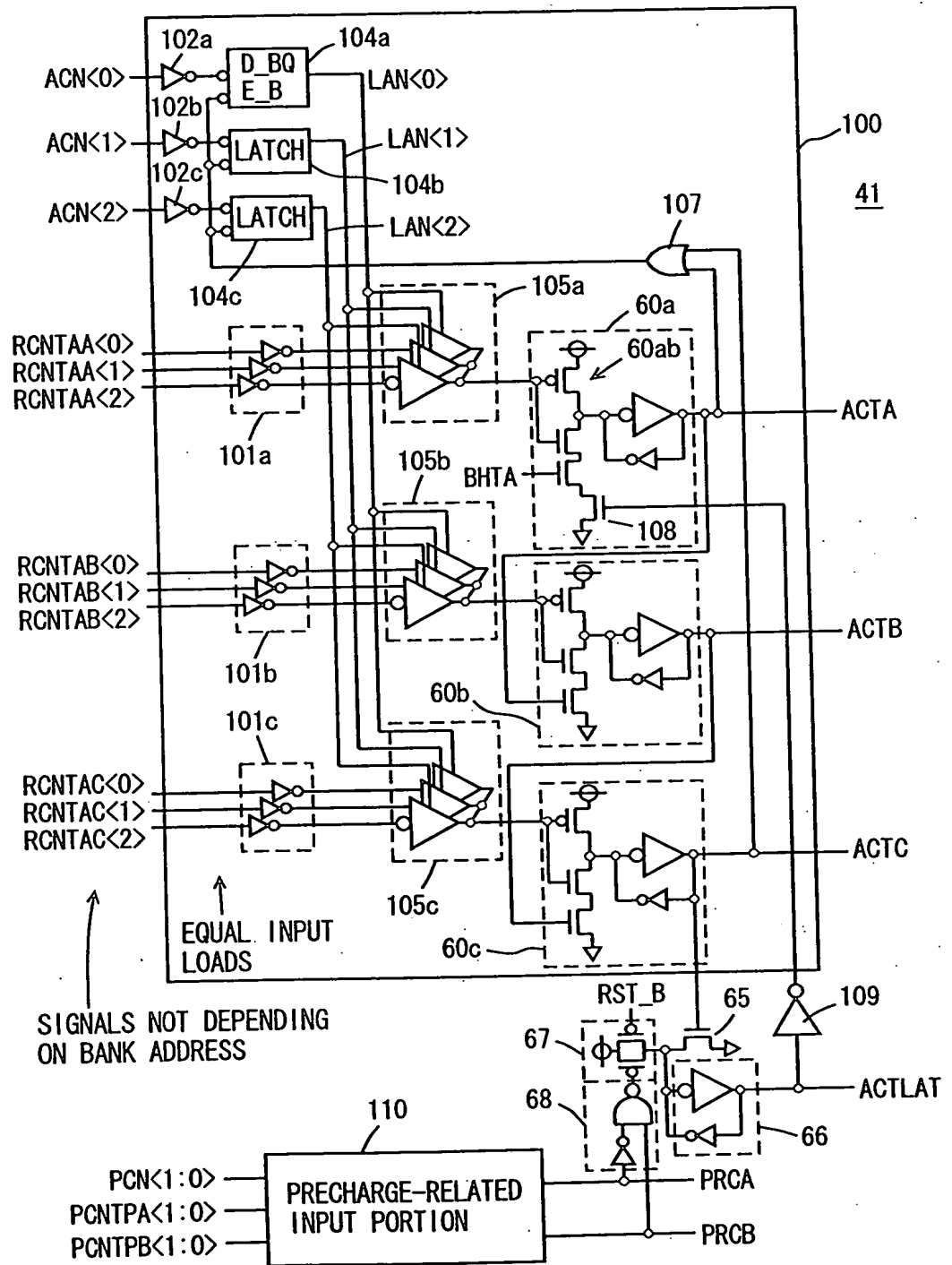


FIG. 33

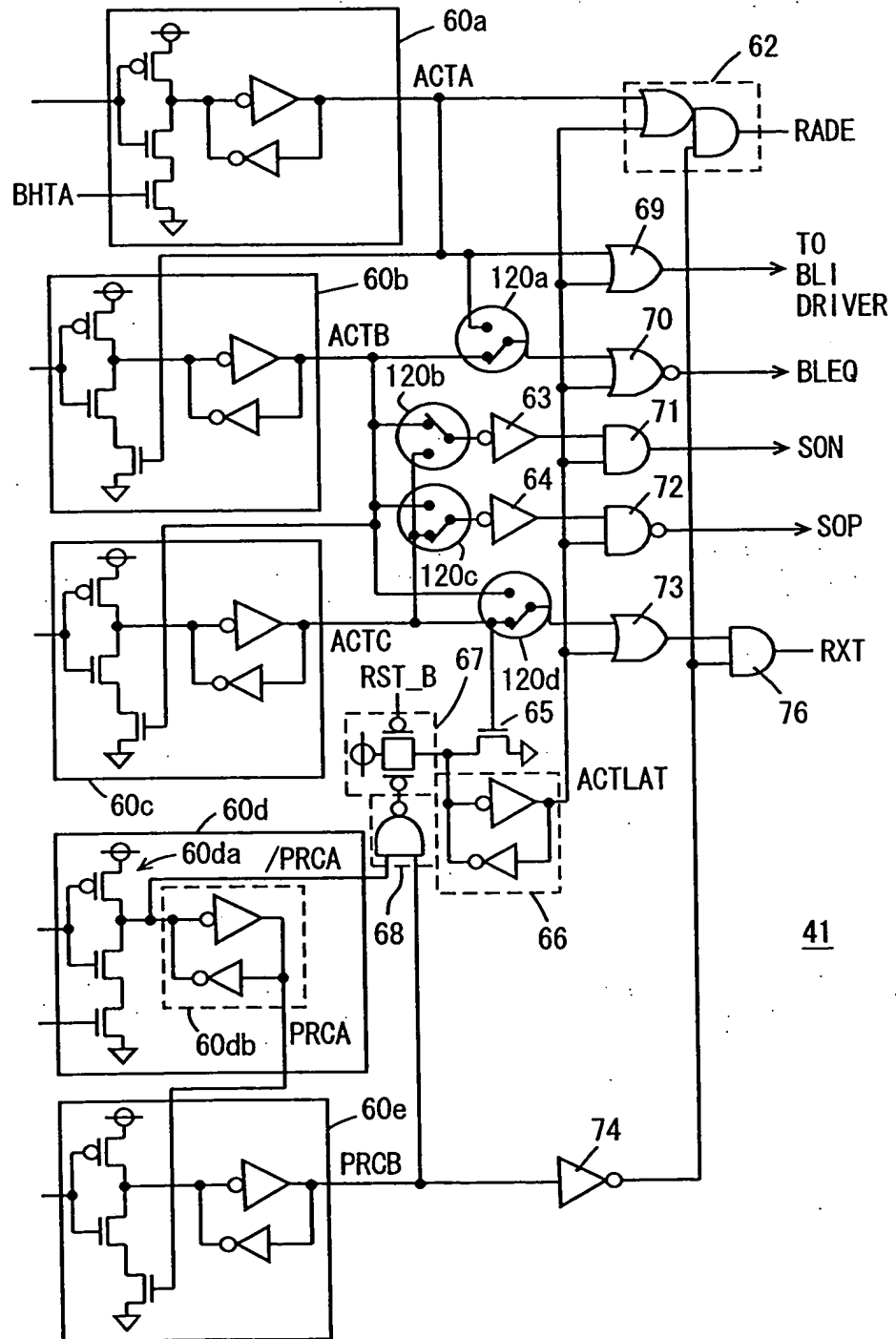
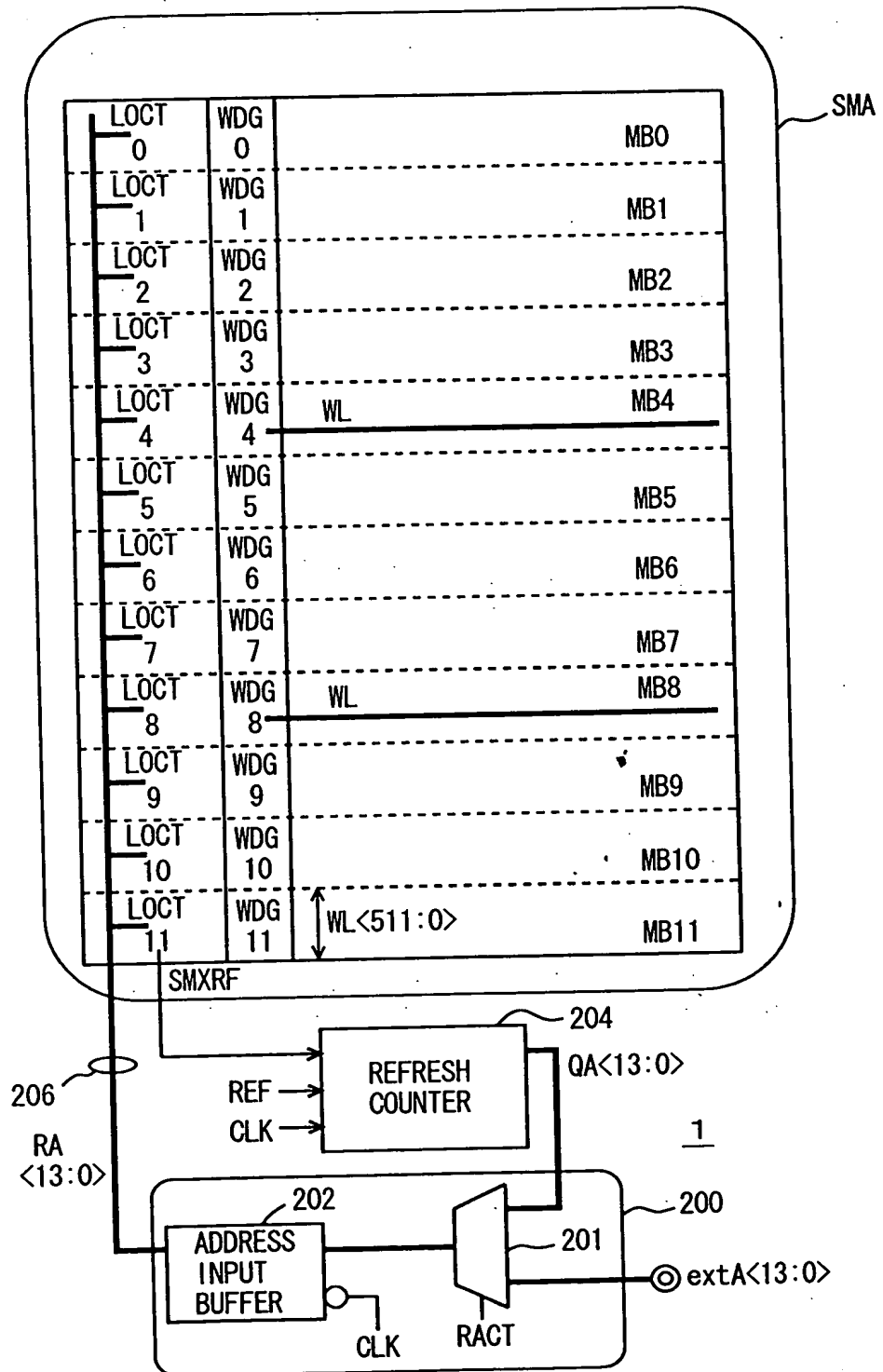


FIG.34



[illegible]

(CORRESPONDING
TO FIG. 3)

FIG.36

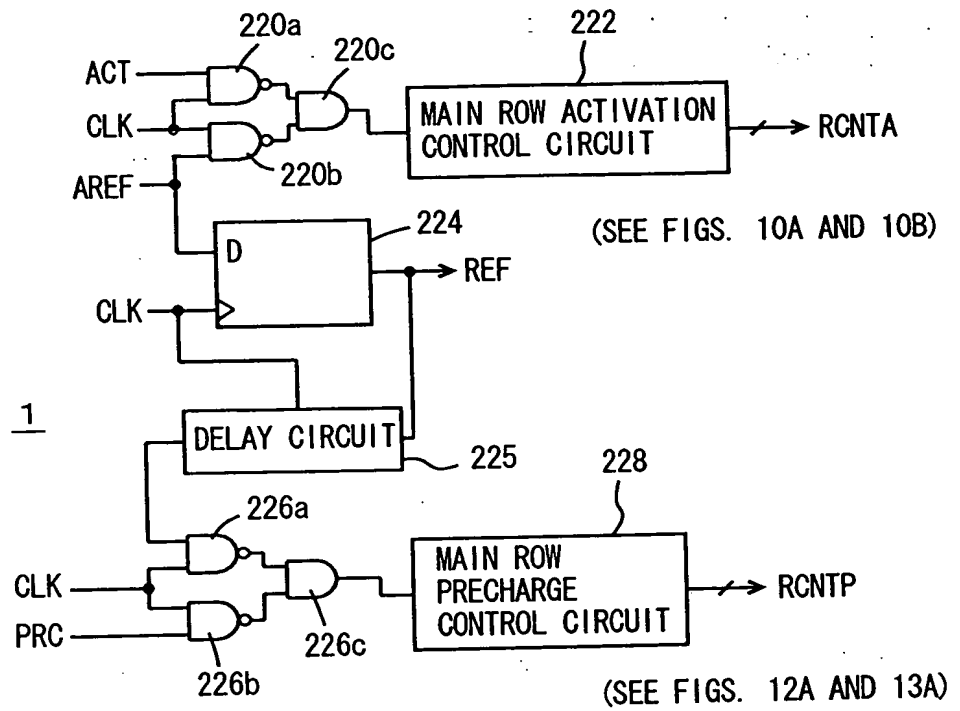


FIG.37

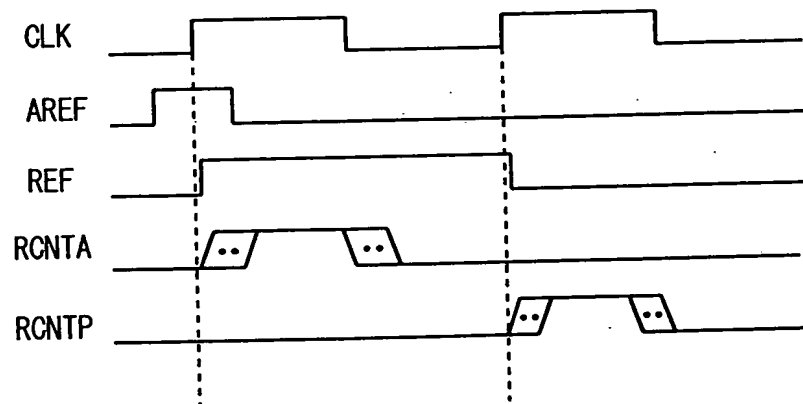


FIG.38

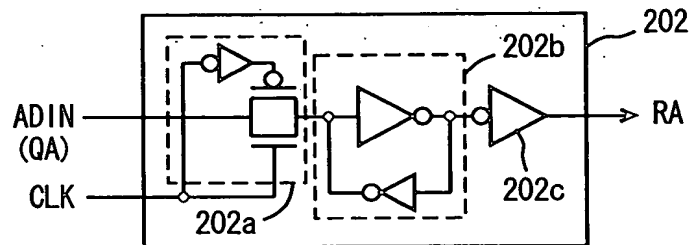


FIG.39

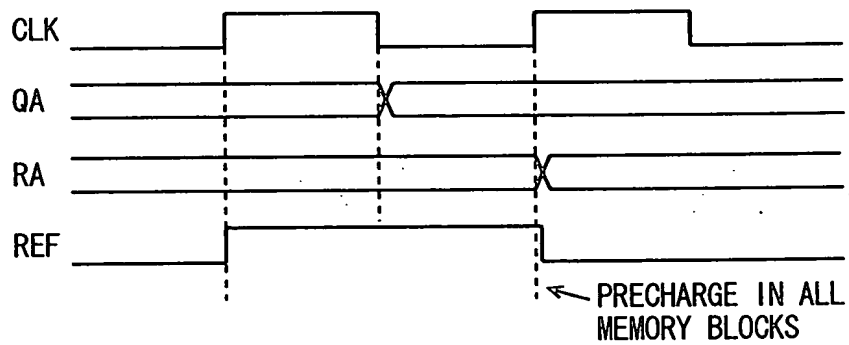


FIG.40

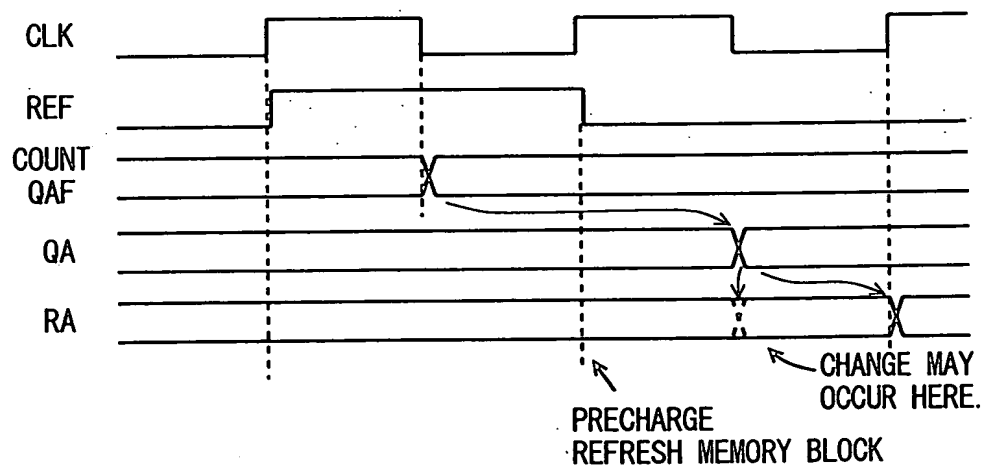


FIG.41

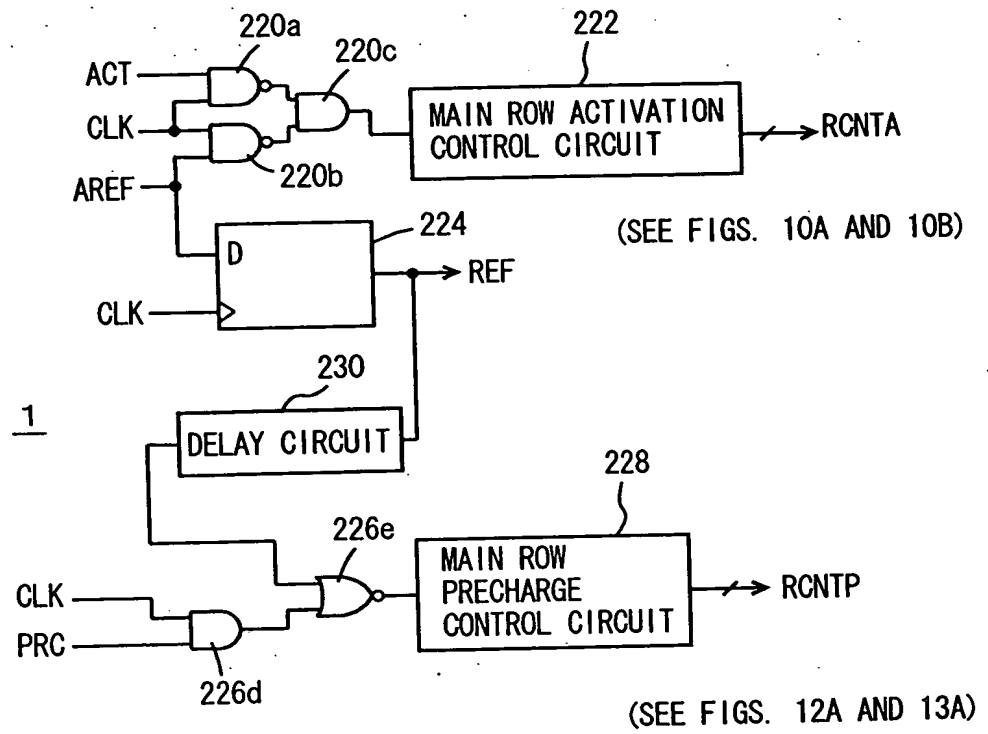


FIG.42

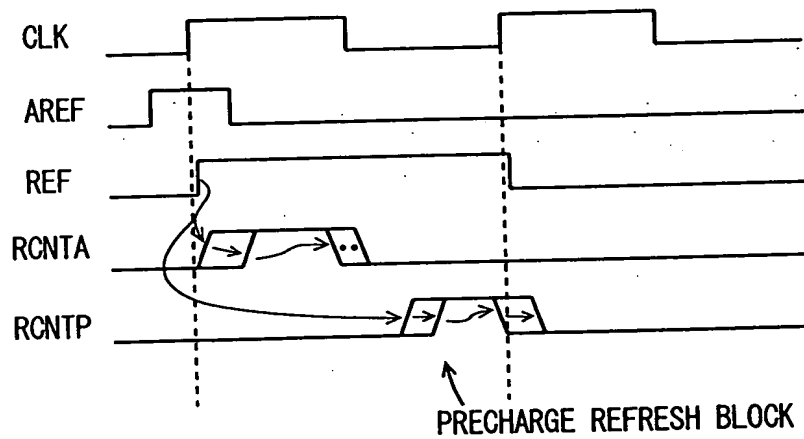


FIG.43

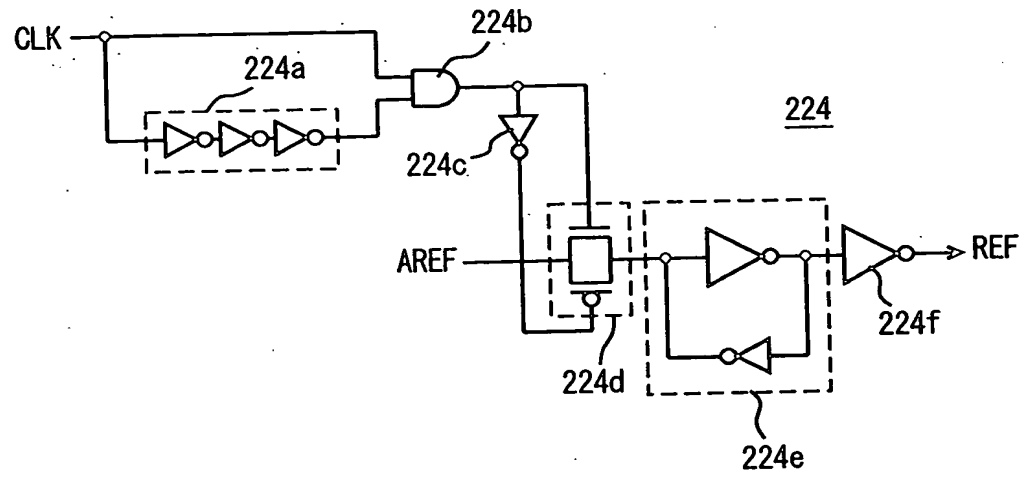


FIG.45

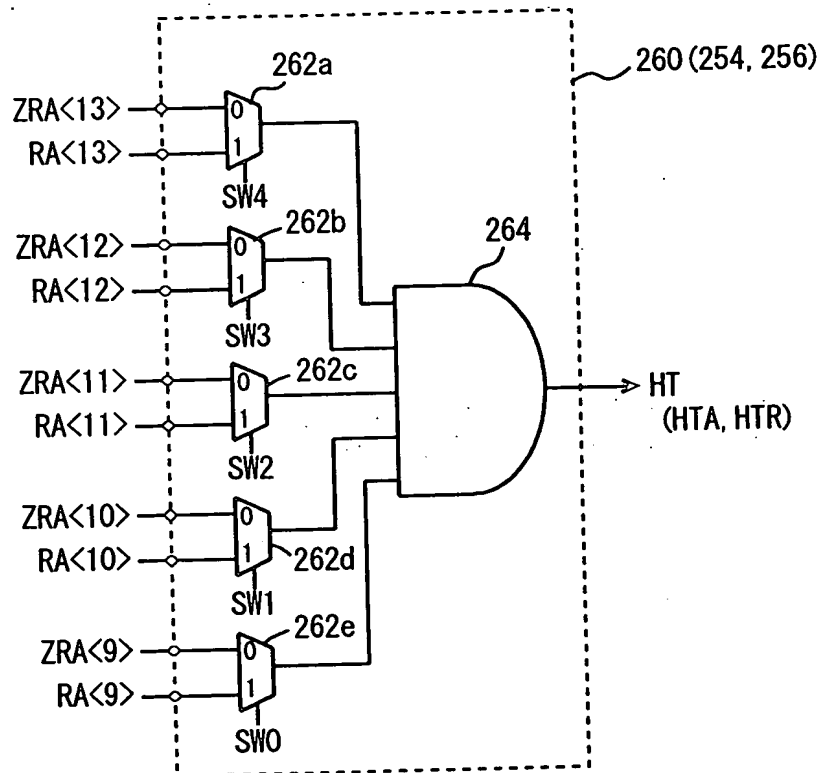


FIG.44

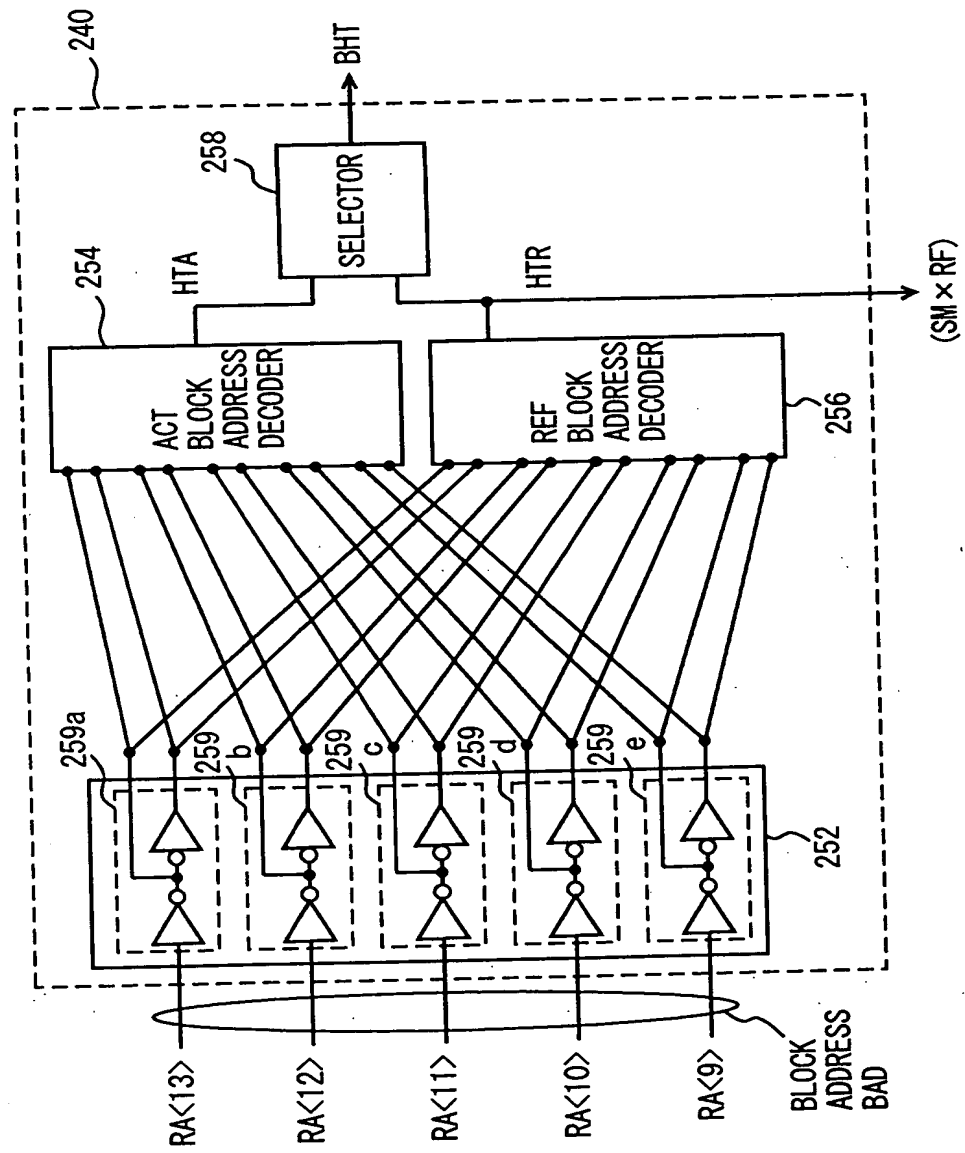


FIG.46

MEMORY BLOCK MB	ACT BLOCK ADDRESS DECODER					REF BLOCK ADDRESS DECODER				
	SW4	SW3	SW2	SW1	SW0	SW4	SW3	SW2	SW1	SW0
0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	1
2	0	0	0	1	0	0	0	0	1	0
3	0	0	0	1	1	0	0	0	1	1
4	0	0	1	0	0	0	0	1	0	0
5	0	0	1	0	1	0	0	1	0	1
6	0	0	1	1	0	0	0	0	0	0
7	0	0	1	1	1	0	0	0	0	1
8	0	1	0	0	0	0	0	0	1	0
9	0	1	0	0	1	0	0	0	1	1
10	0	1	0	1	0	0	0	1	0	0
11	0	1	0	1	1	0	0	1	0	1

FIG.47

MEMORY BLOCK MB	ACT BLOCK ADDRESS DECODER					REF BLOCK ADDRESS DECODER				
	SW4	SW3	SW2	SW1	SW0	SW4	SW3	SW2	SW1	SW0
0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	1
2	0	0	0	1	0	0	0	0	0	0
3	0	0	0	1	1	0	0	0	0	1
4	0	0	1	0	0	0	0	0	0	0
5	0	0	1	0	1	0	0	0	0	1

FIG.48A

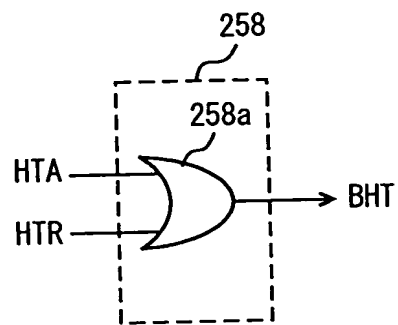


FIG.48B

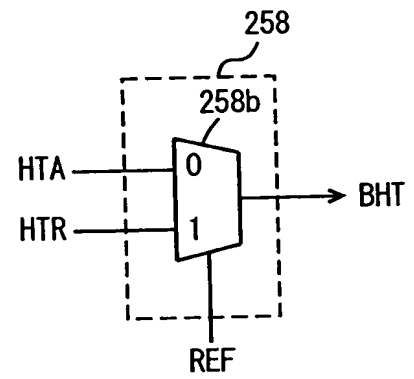


FIG.48C

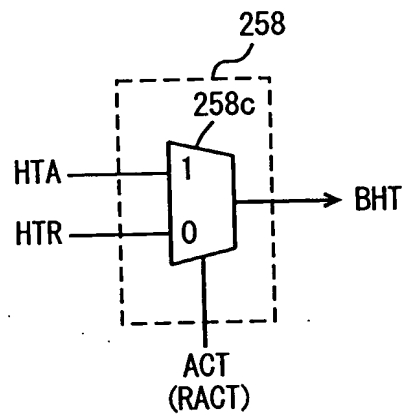


FIG.49

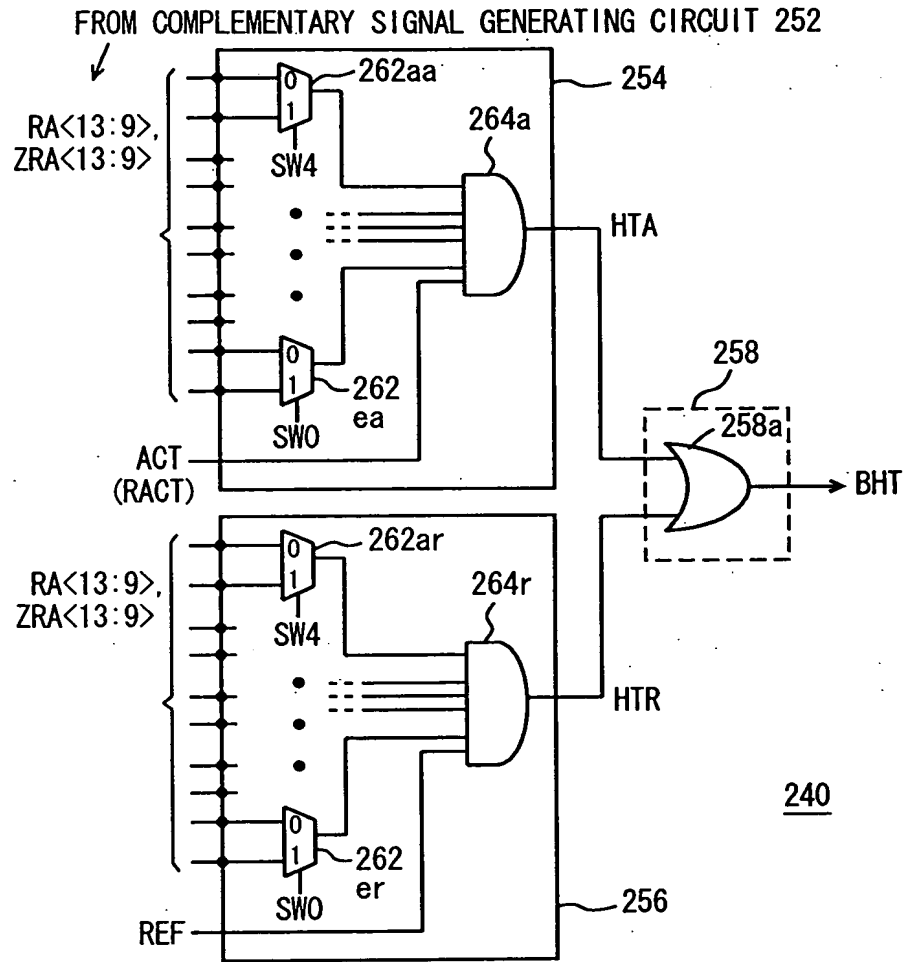


FIG.50

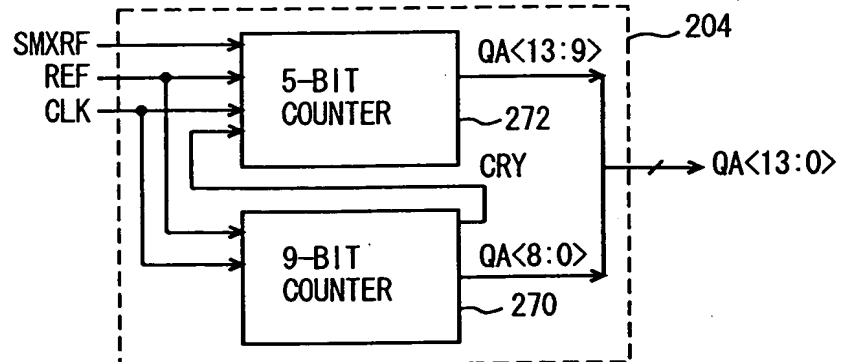


FIG.51

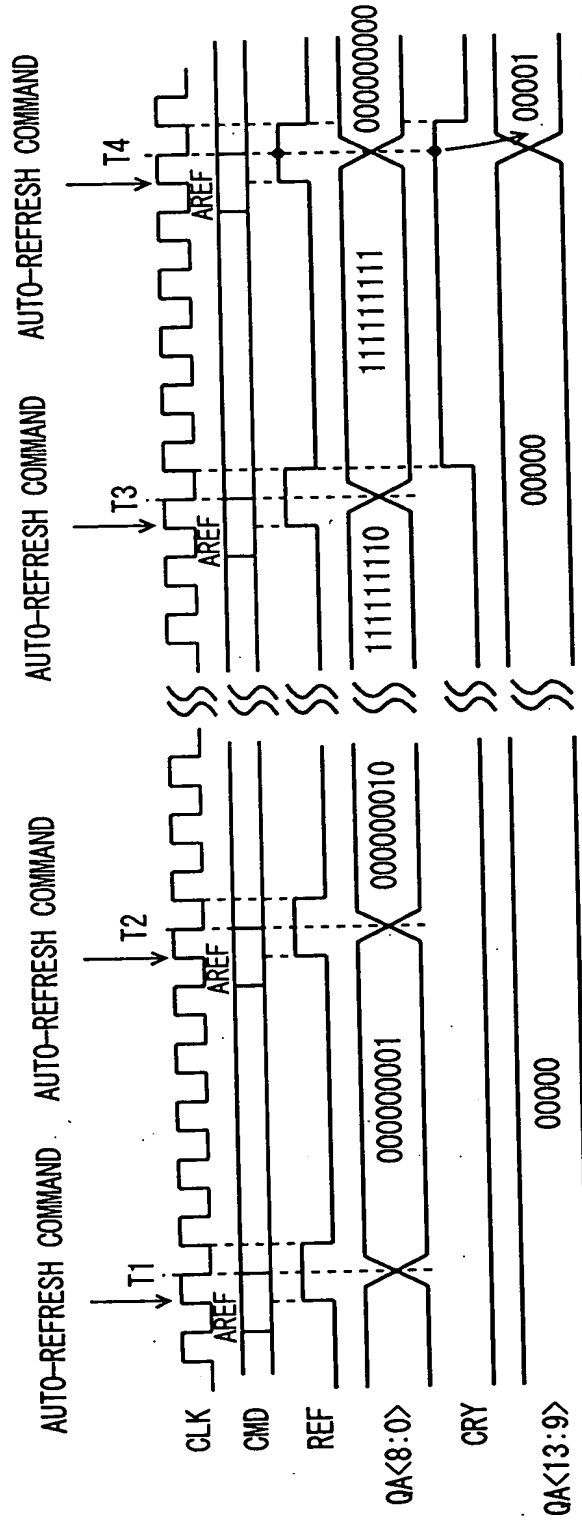


FIG.52

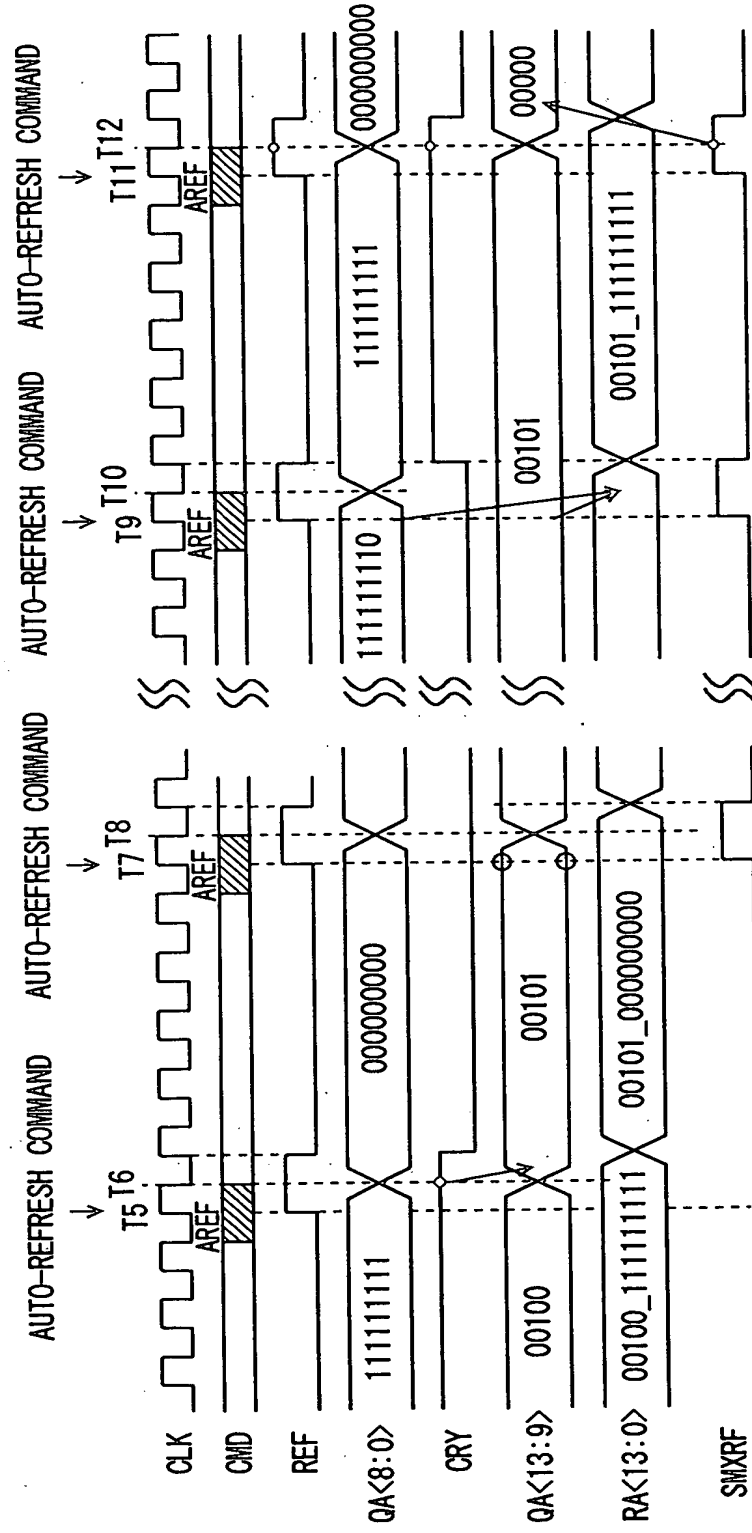


FIG.53

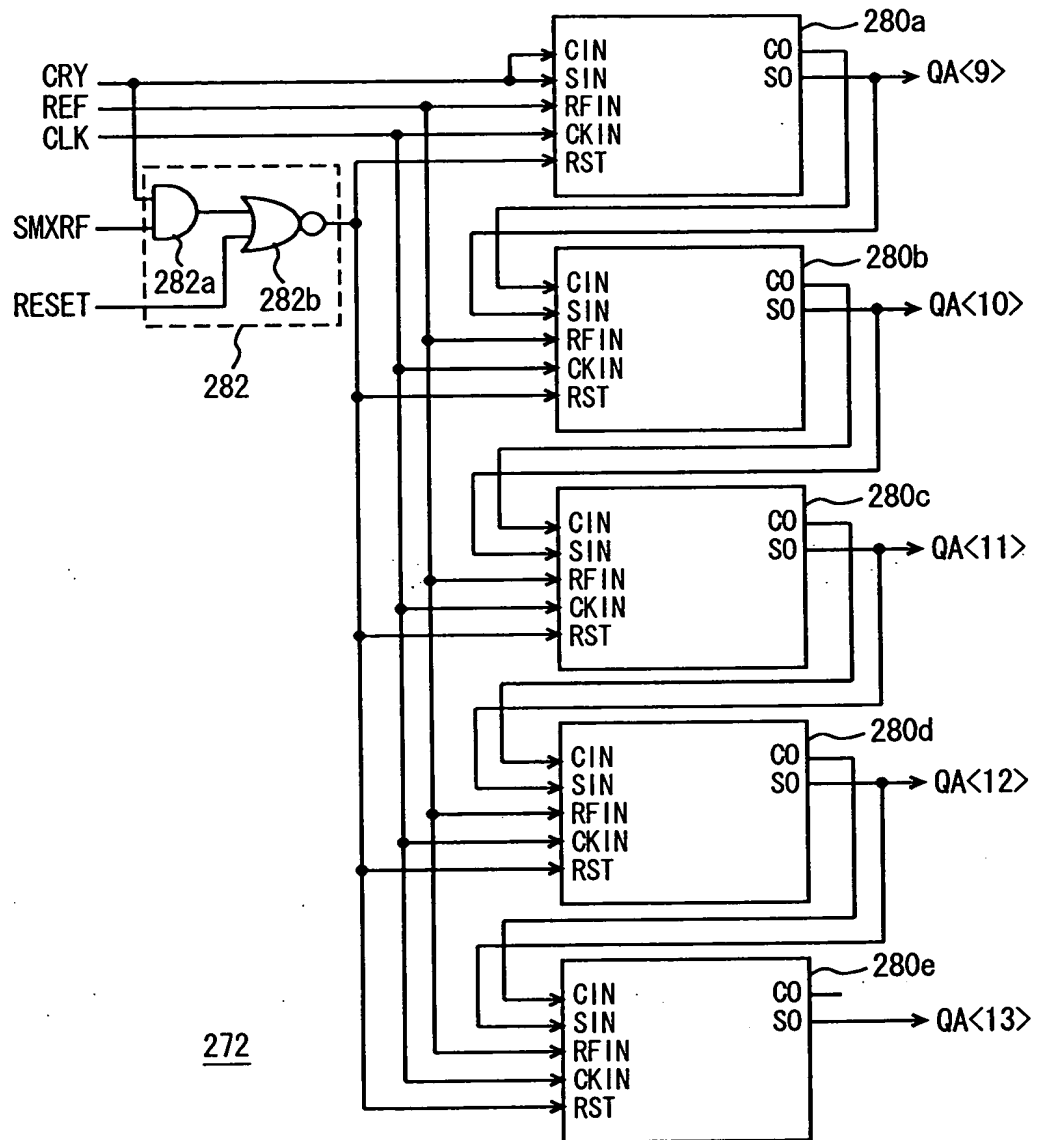


FIG.54

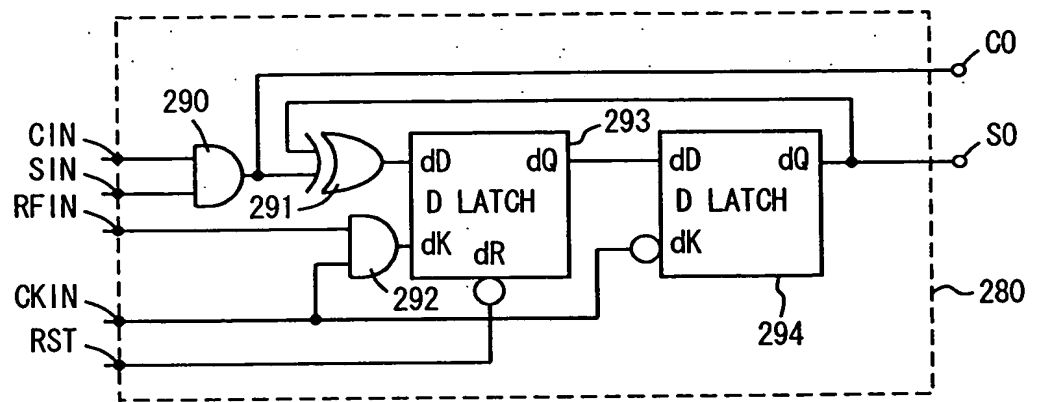


FIG.55

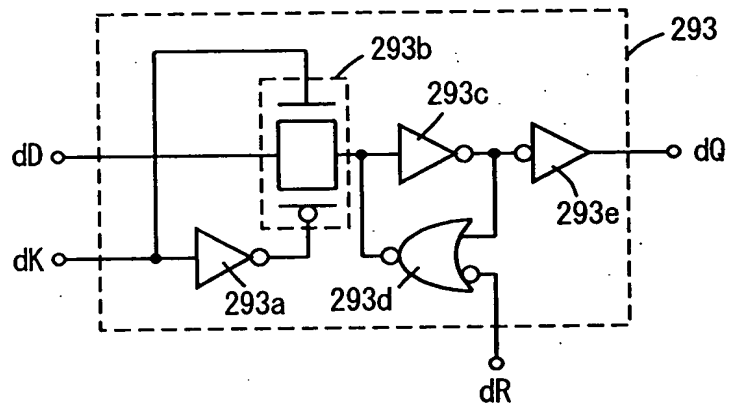


FIG.56

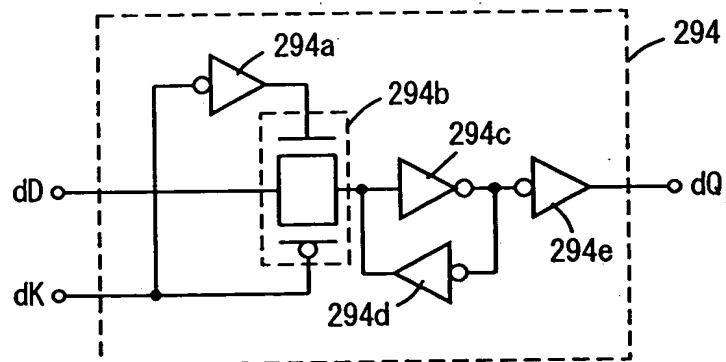


FIG.57

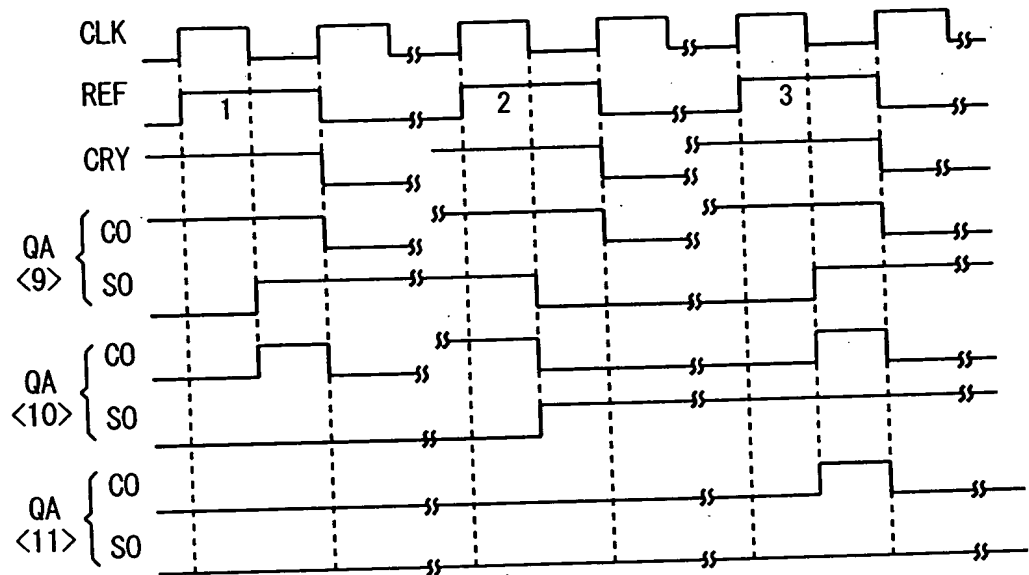


FIG.58

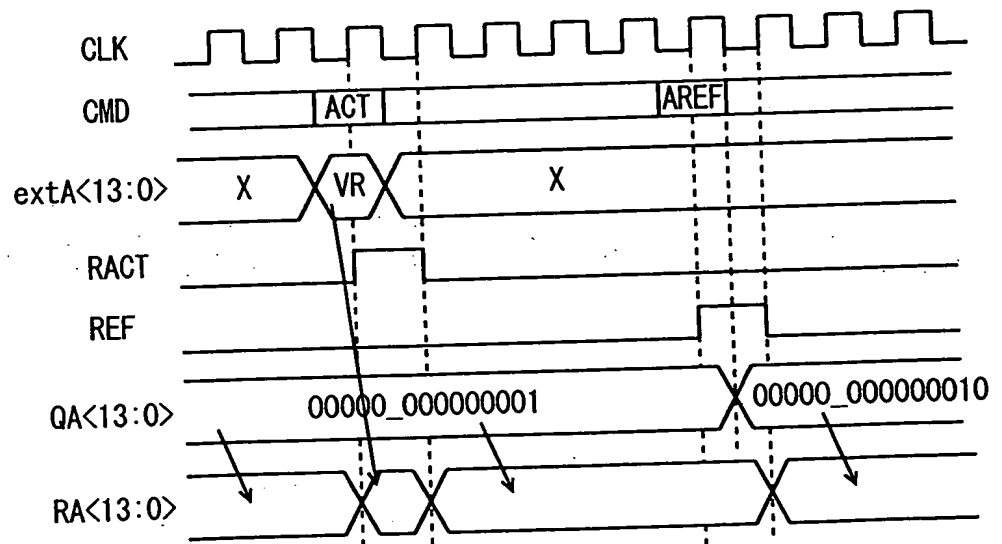


FIG.59

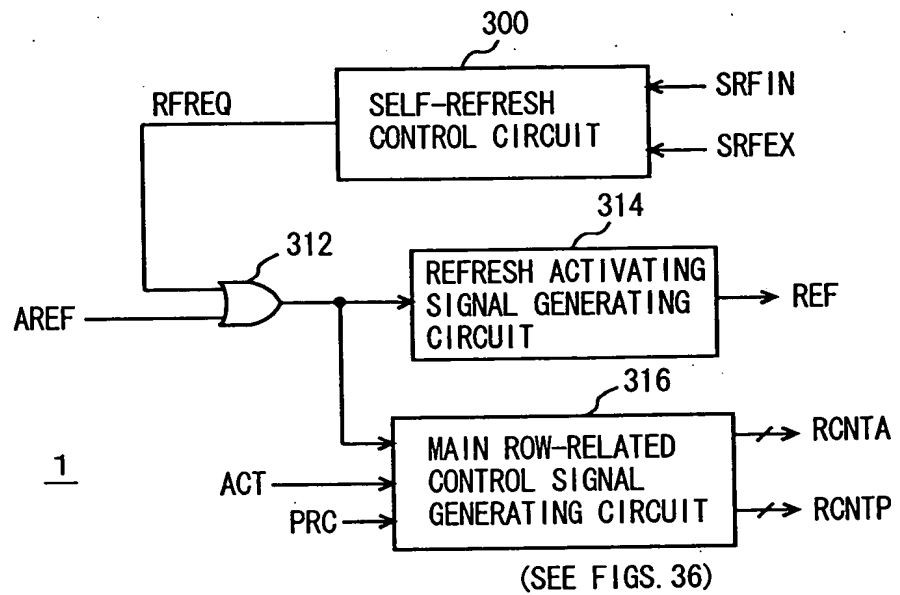


FIG.60

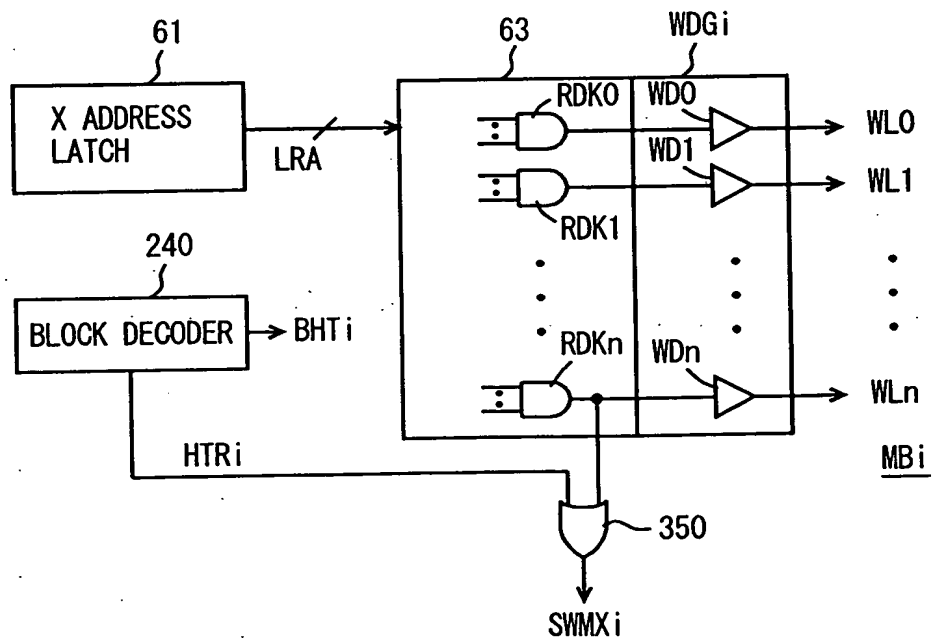


FIG.61

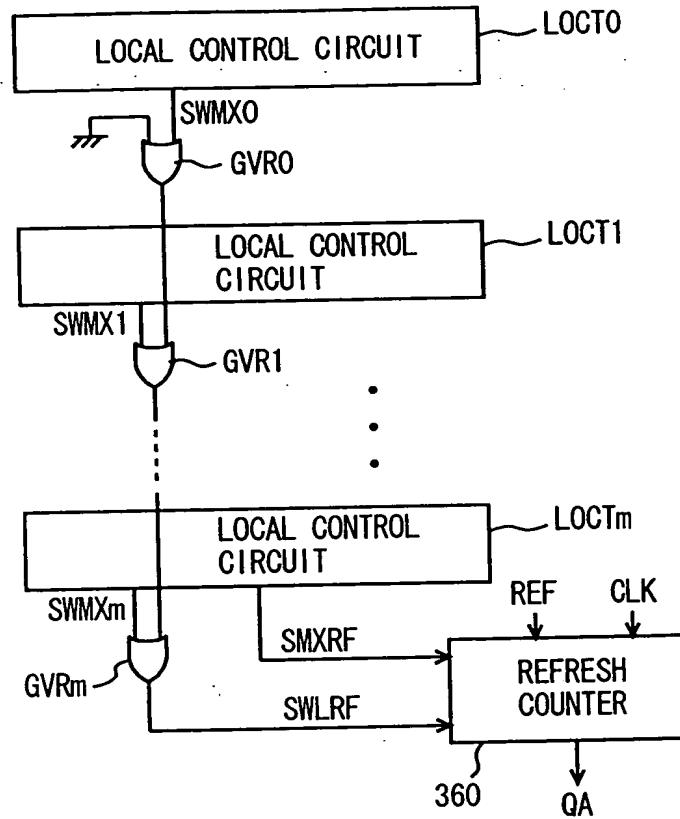


FIG.62

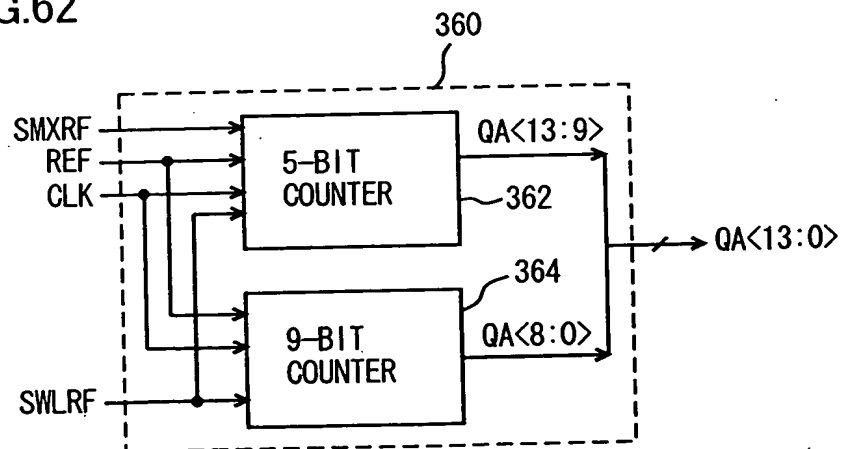
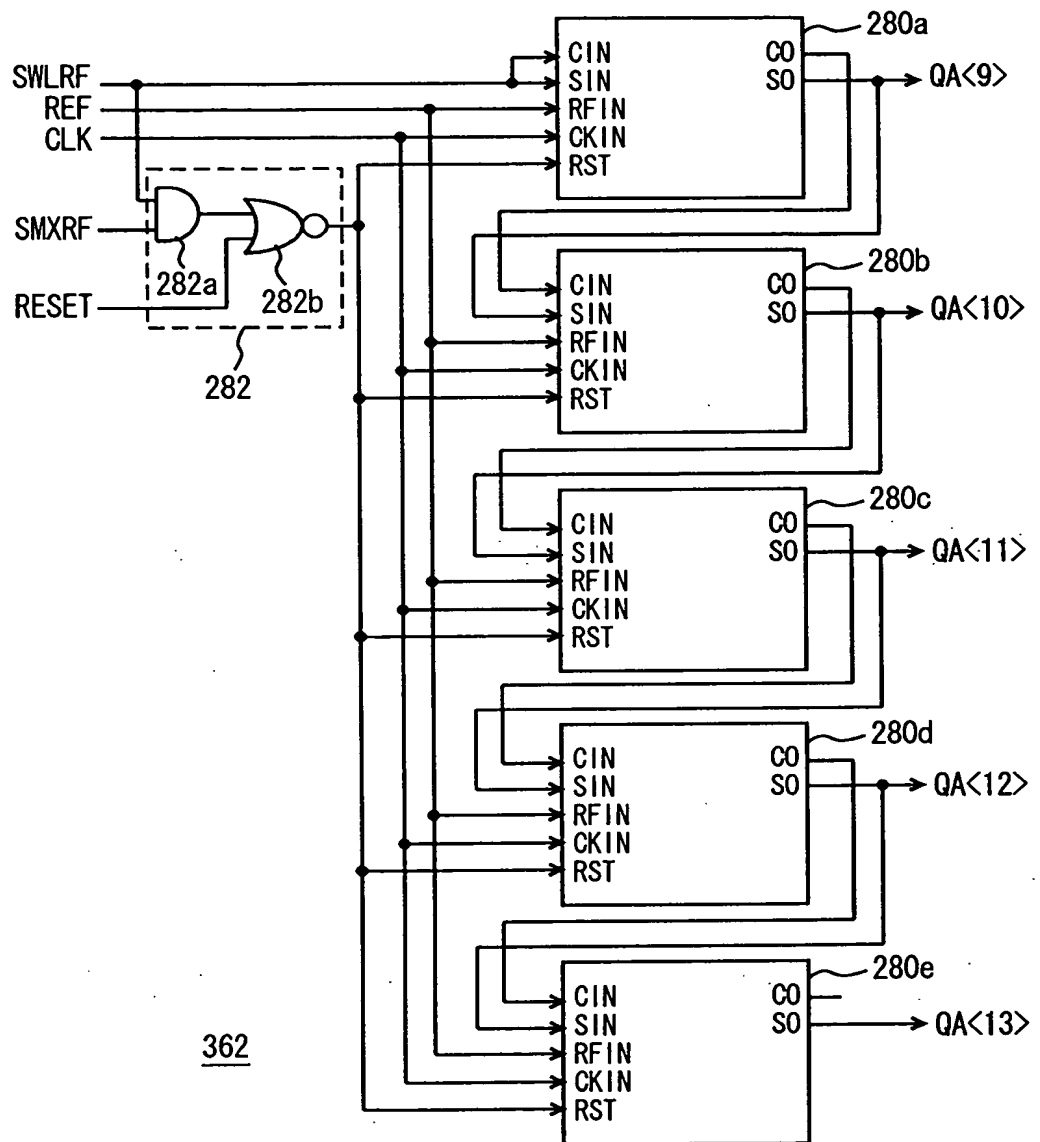


FIG.63



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FIG.64

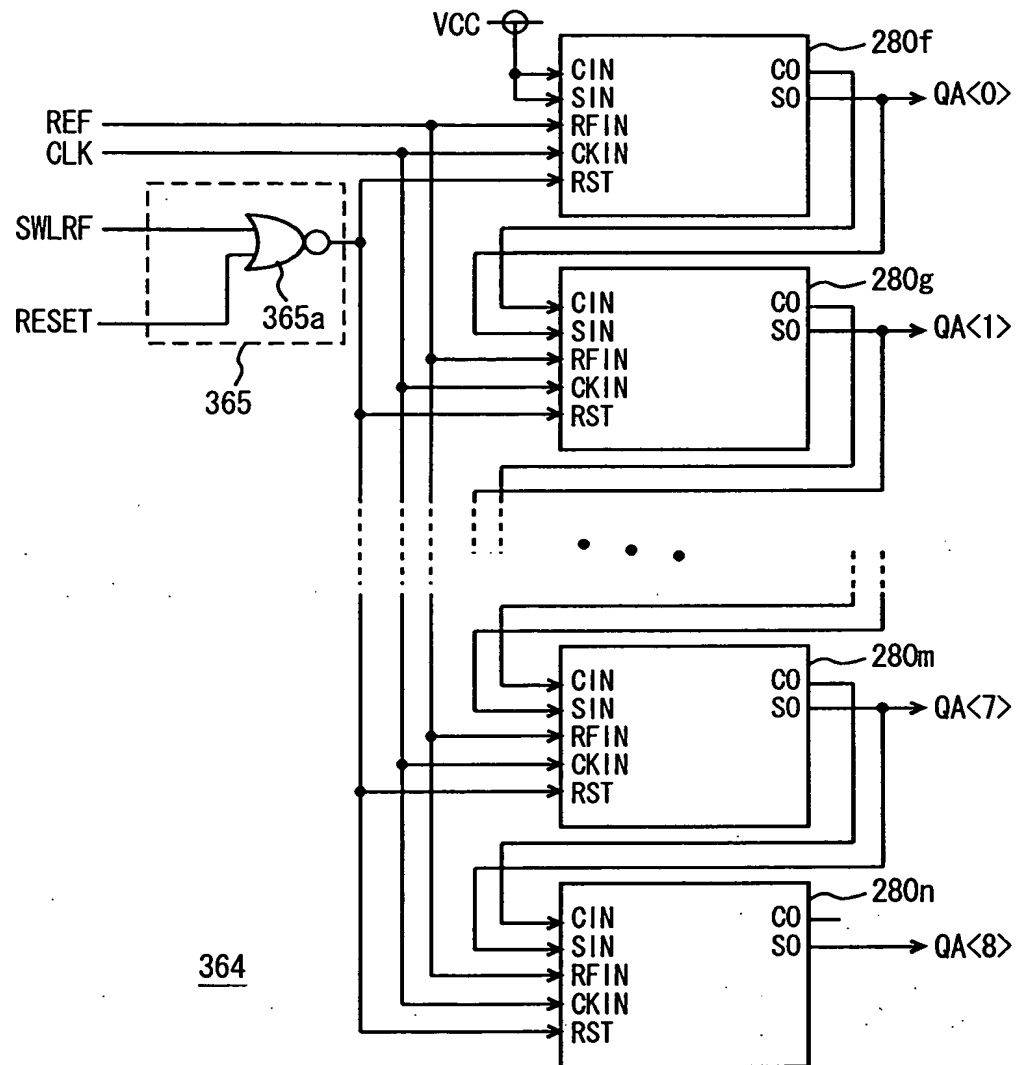


FIG.65

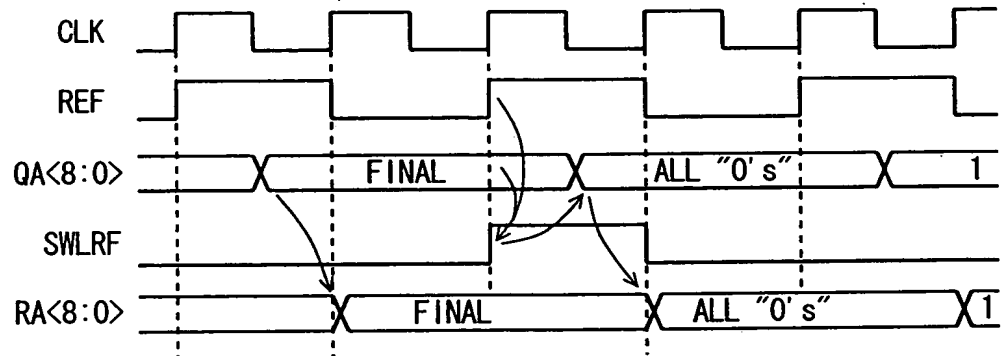


FIG.66

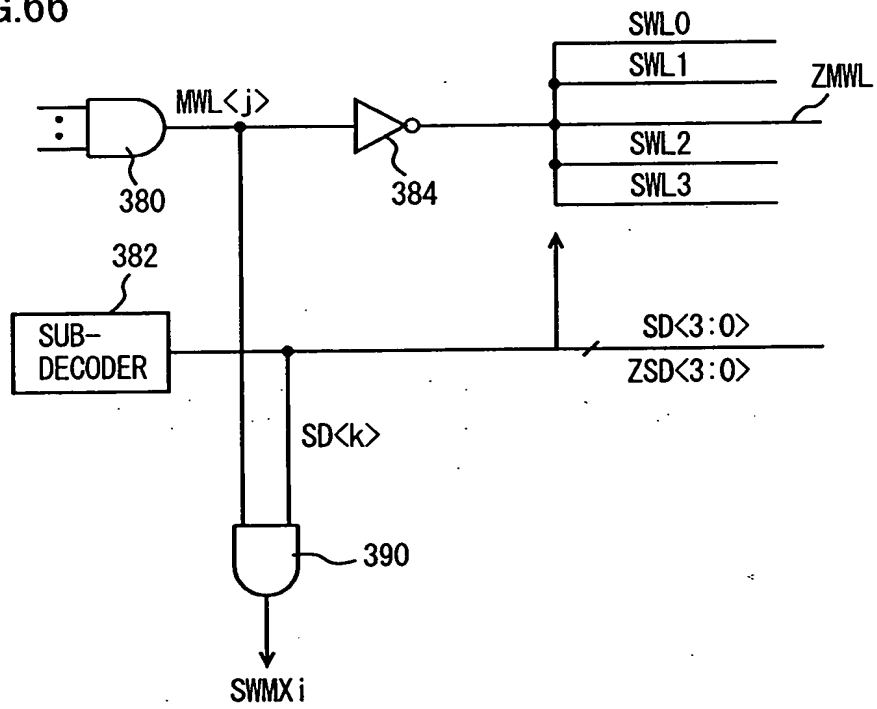


FIG.67

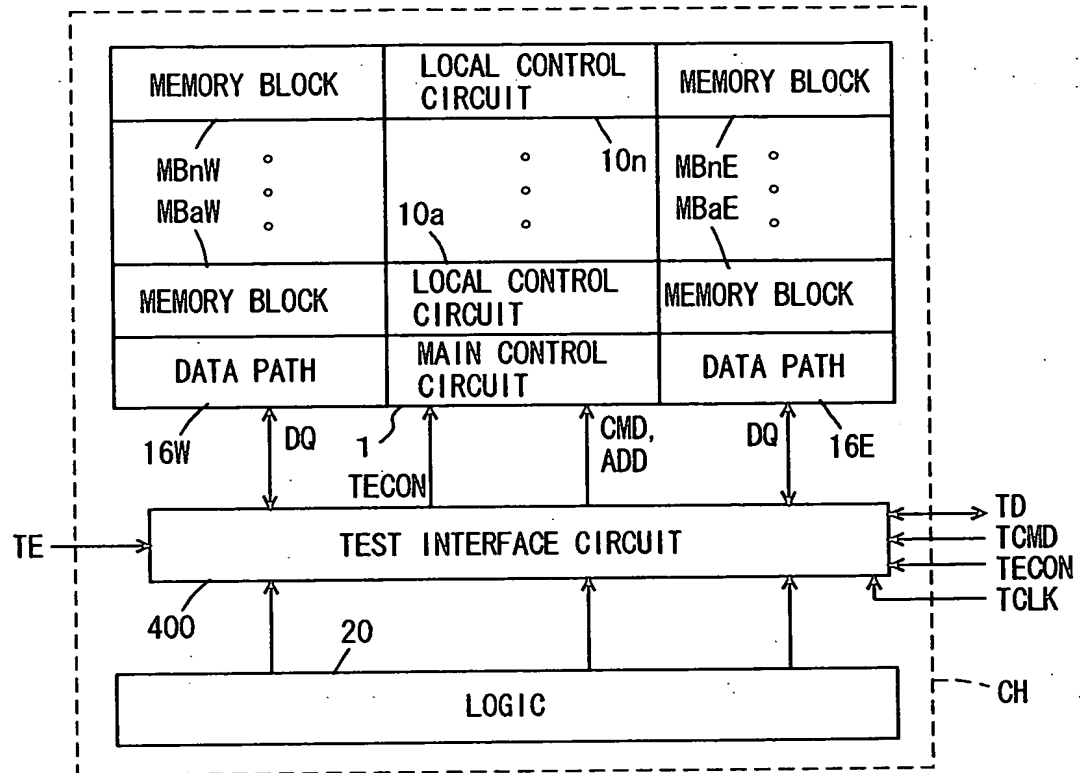


FIG.68

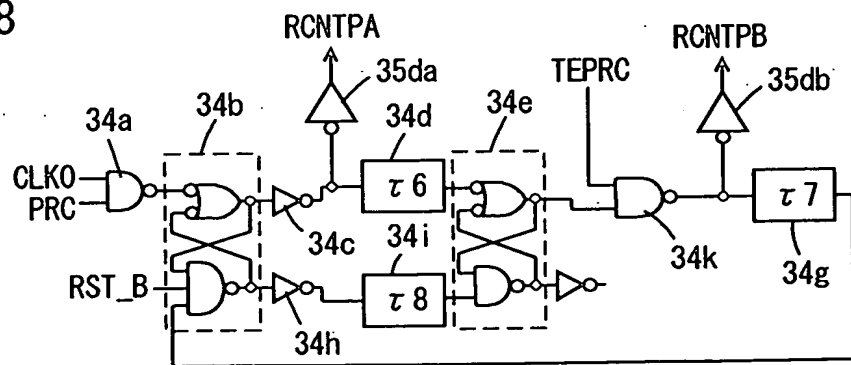


FIG.69

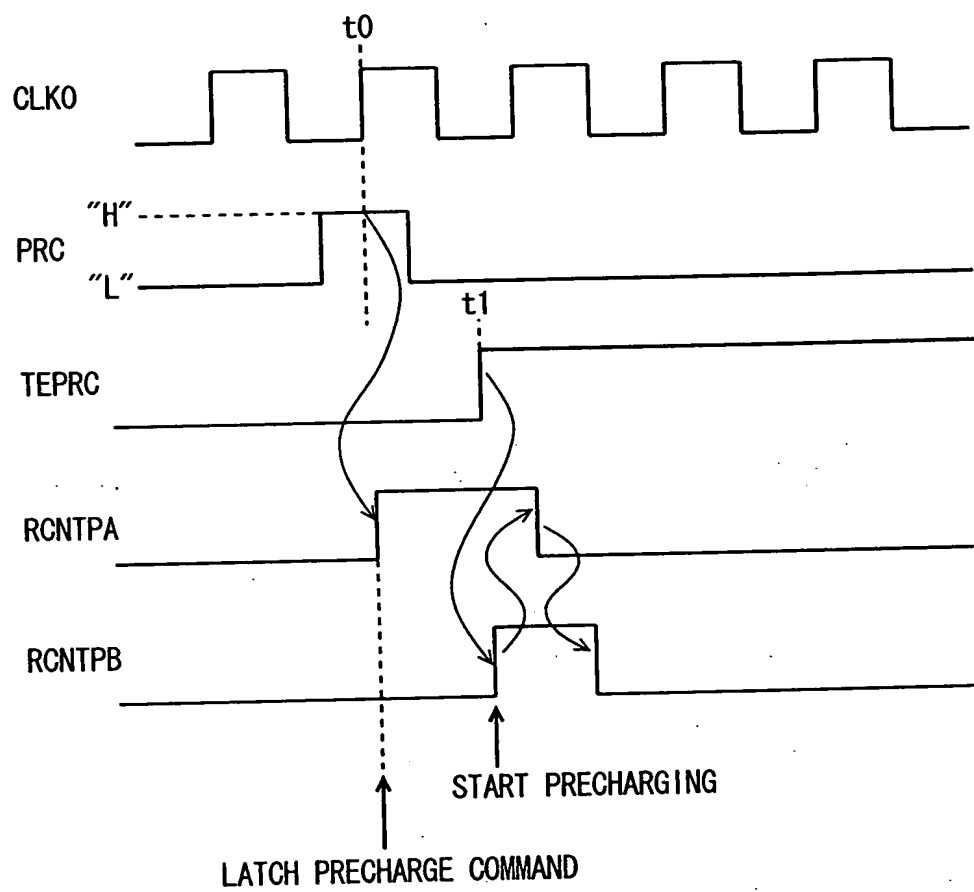


FIG.70

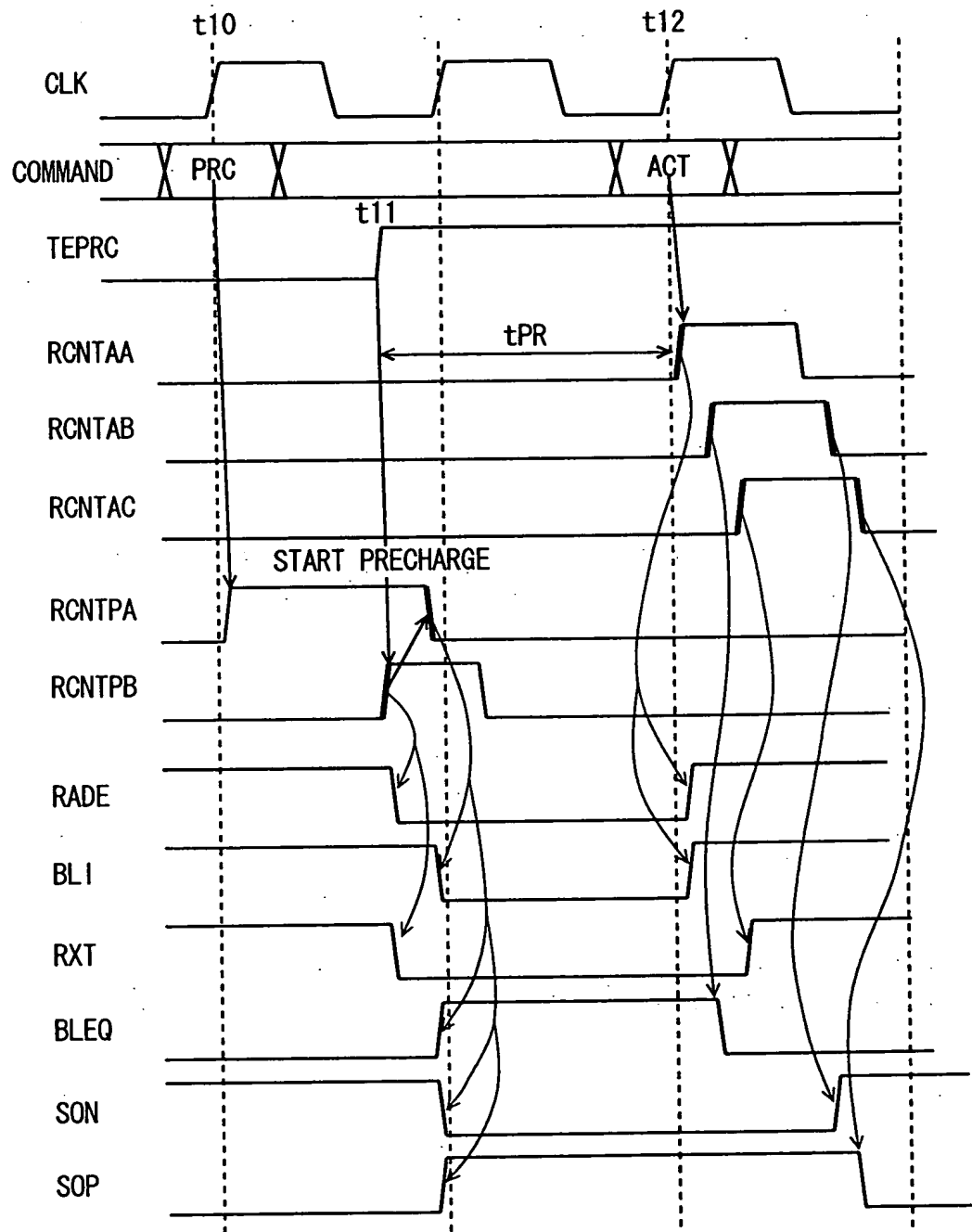


FIG.71

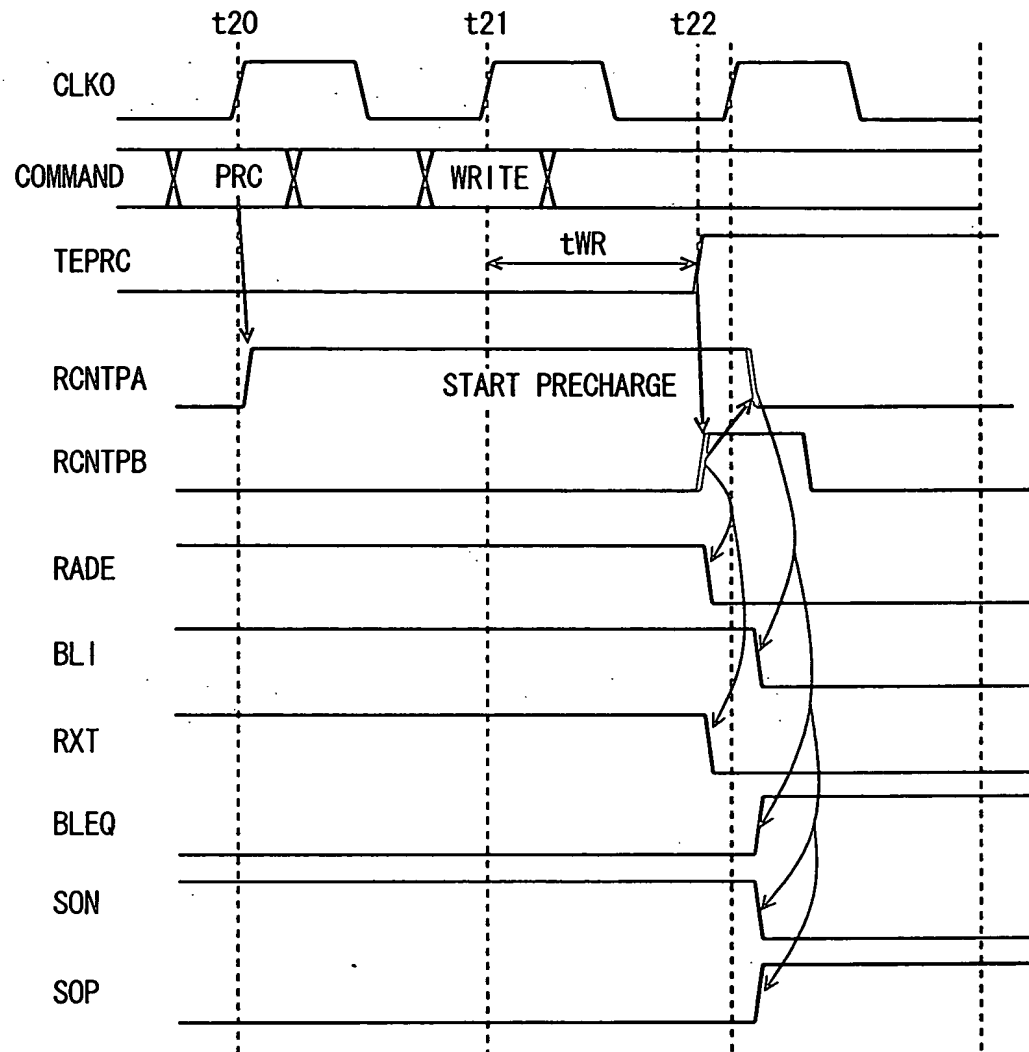


FIG.72

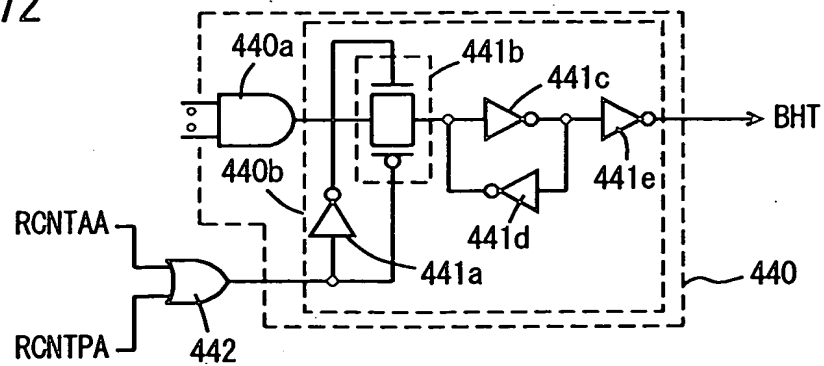


FIG.73

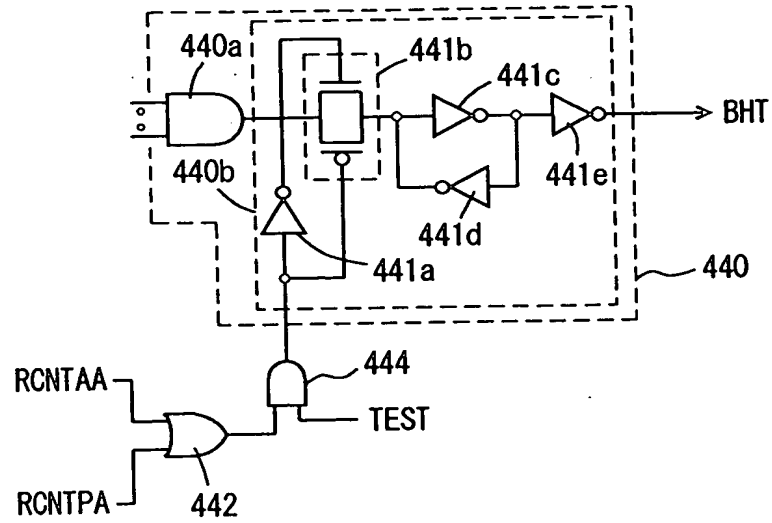


FIG.74

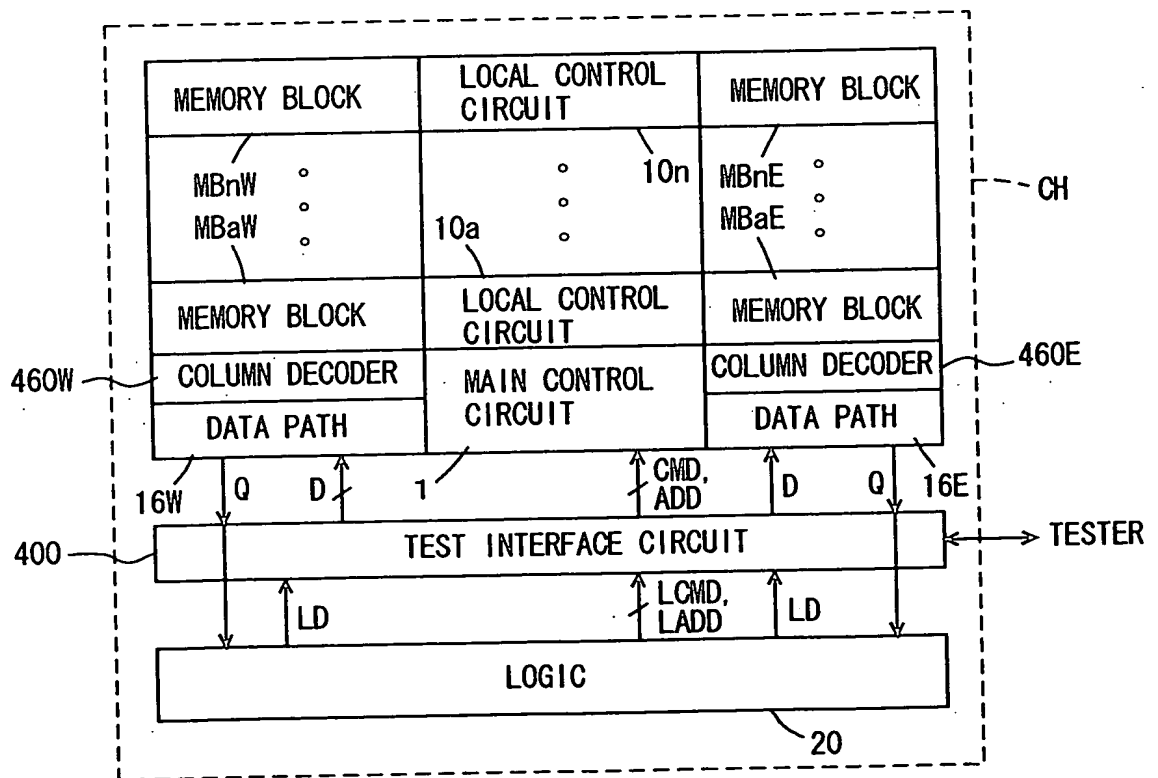


FIG.75

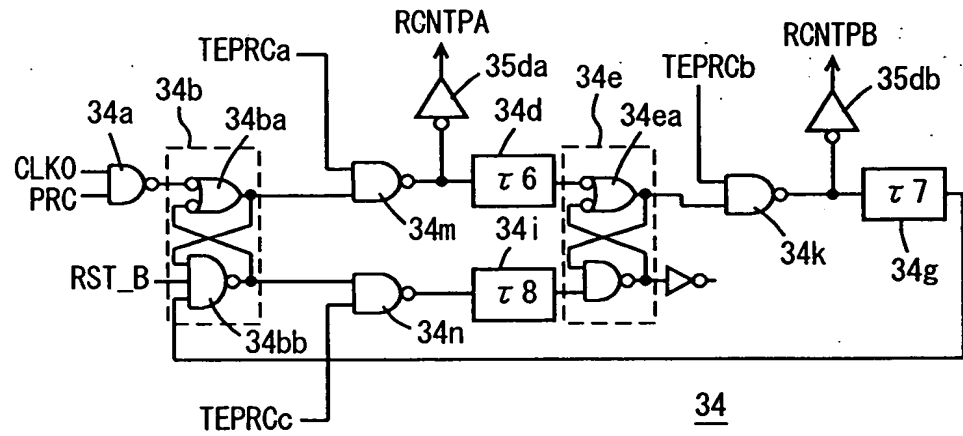


FIG.76

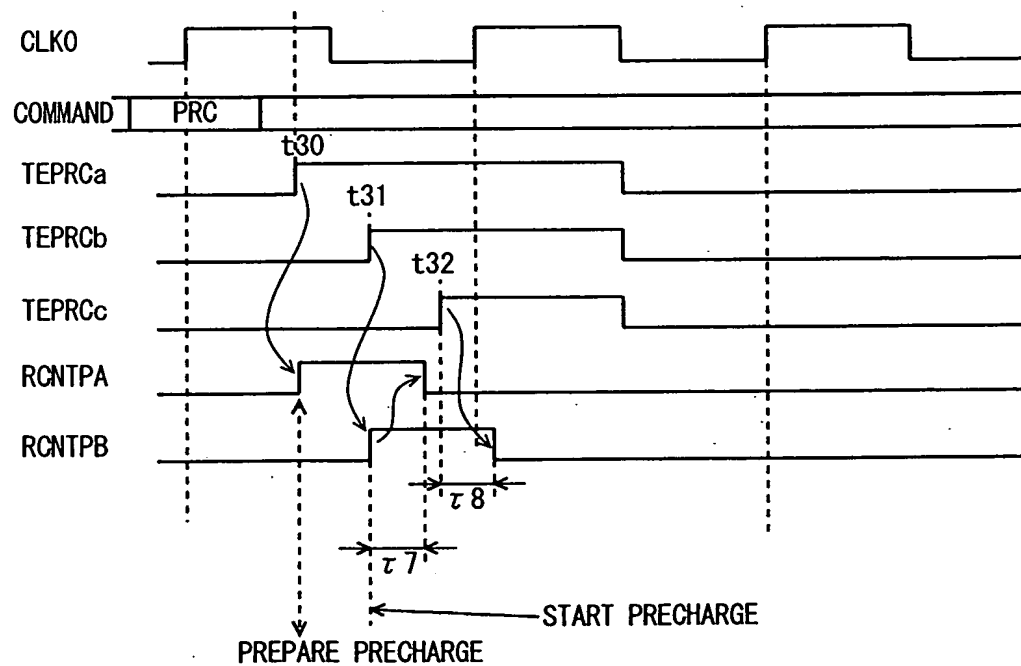


FIG.77

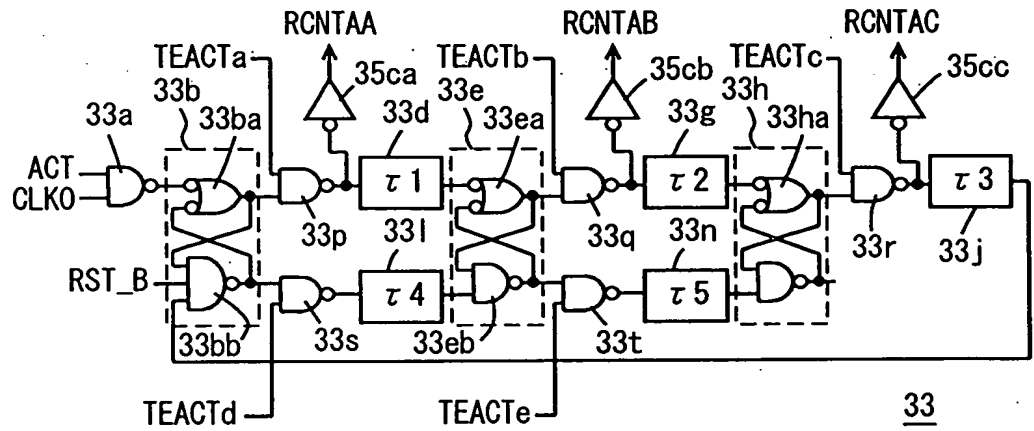


FIG.78

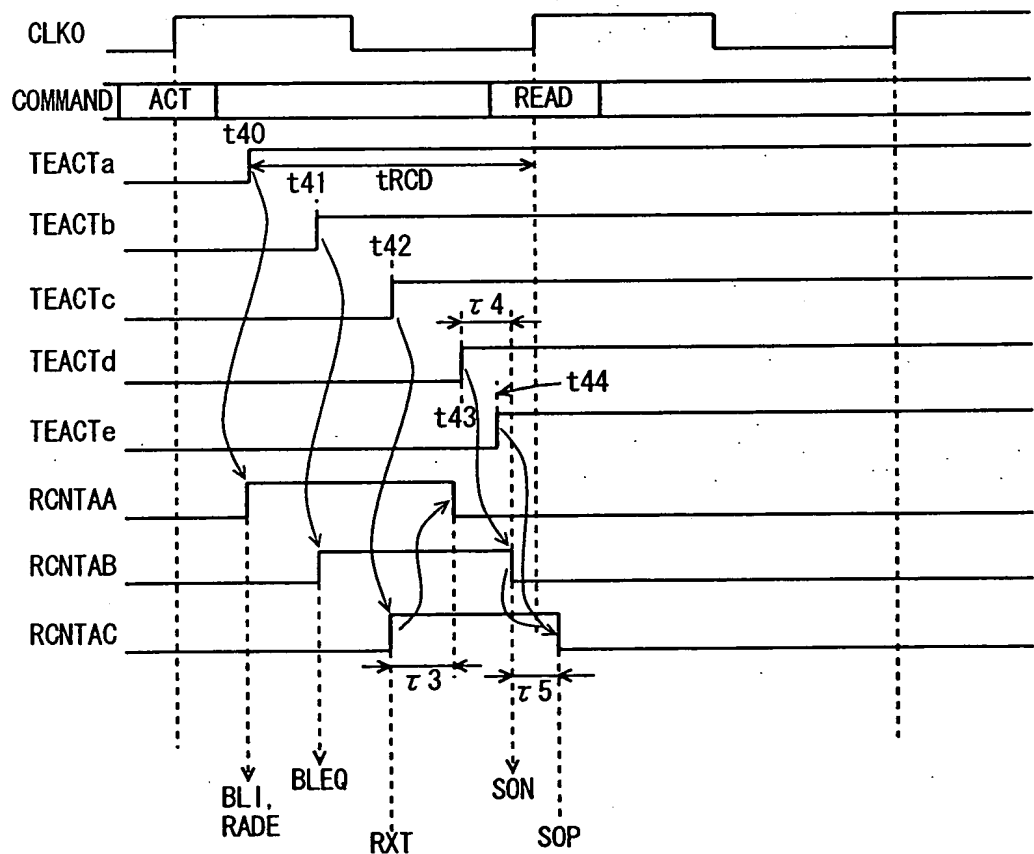


FIG.79 PRIOR ART

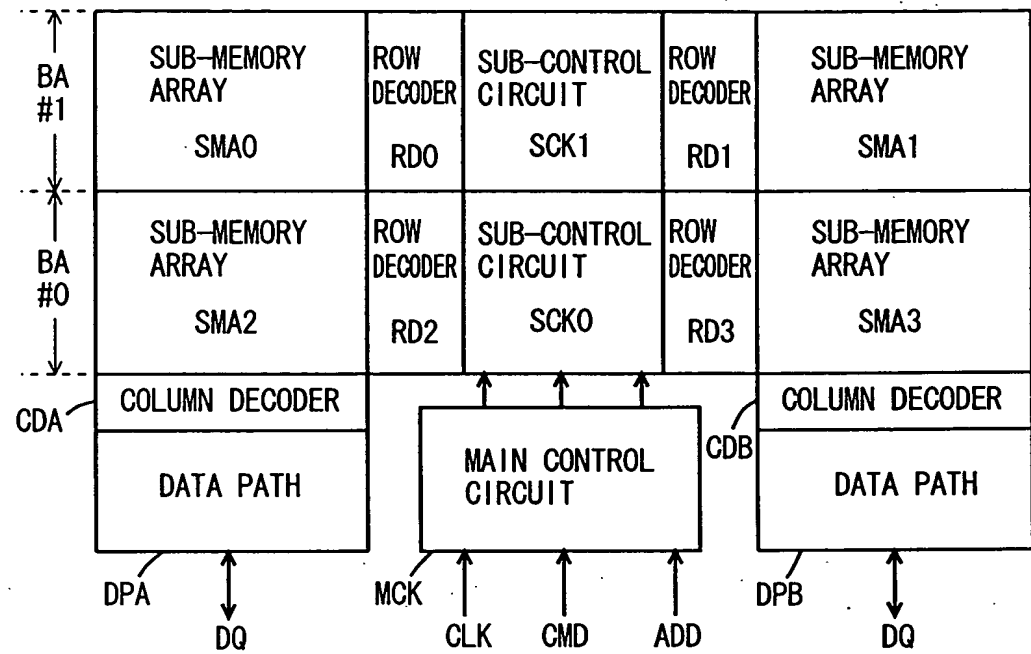


FIG.80 PRIOR ART

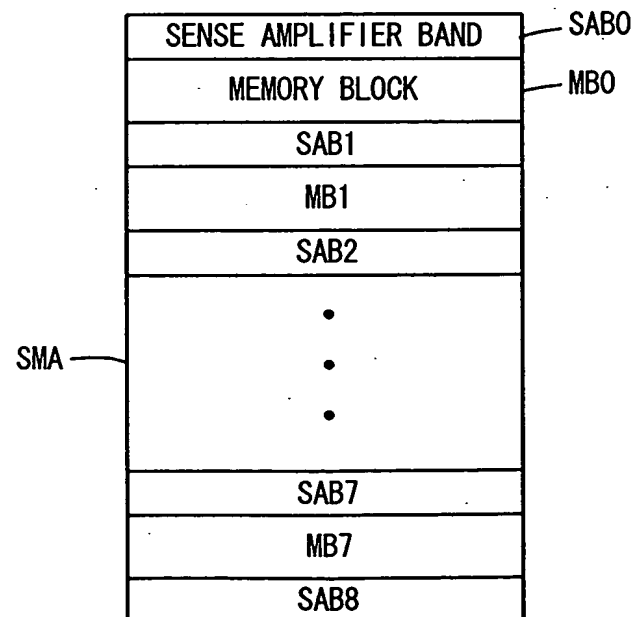


FIG.81 PRIOR ART

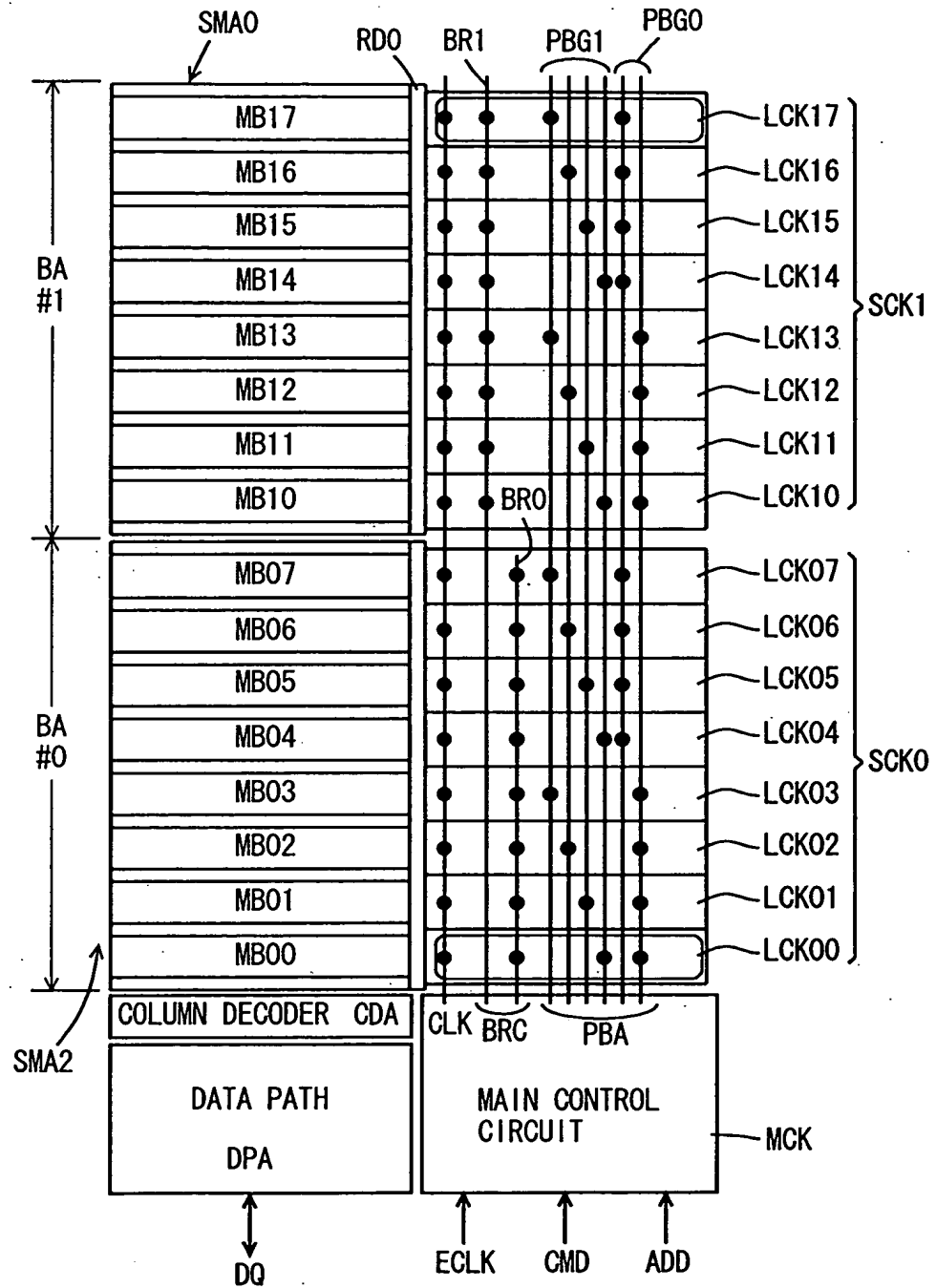


FIG.82 PRIOR ART

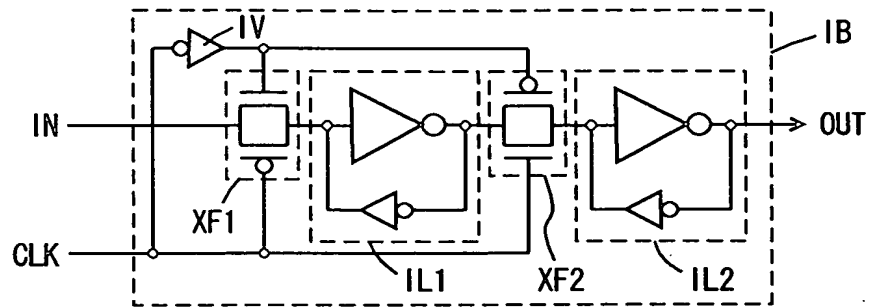


FIG.83 PRIOR ART

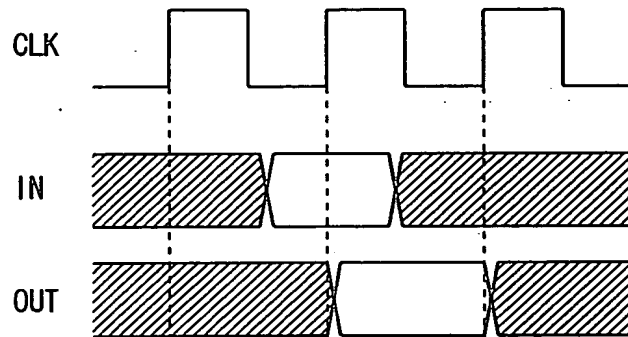


FIG.84 PRIOR ART

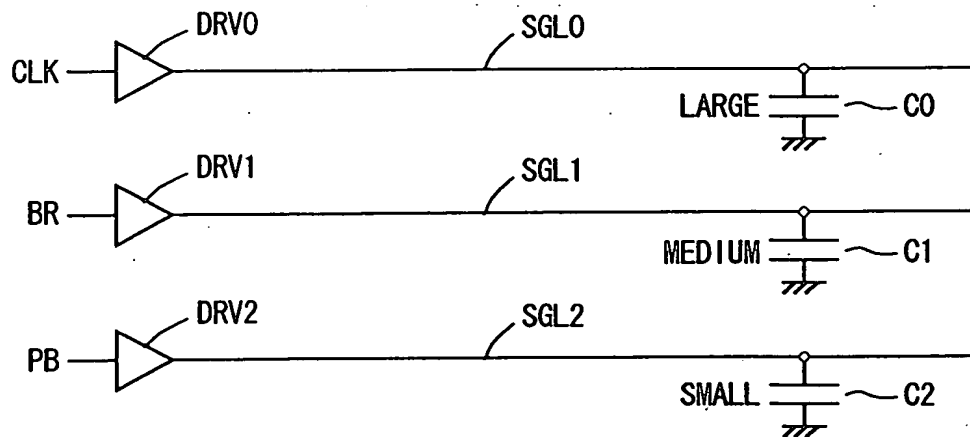


FIG.85 PRIOR ART

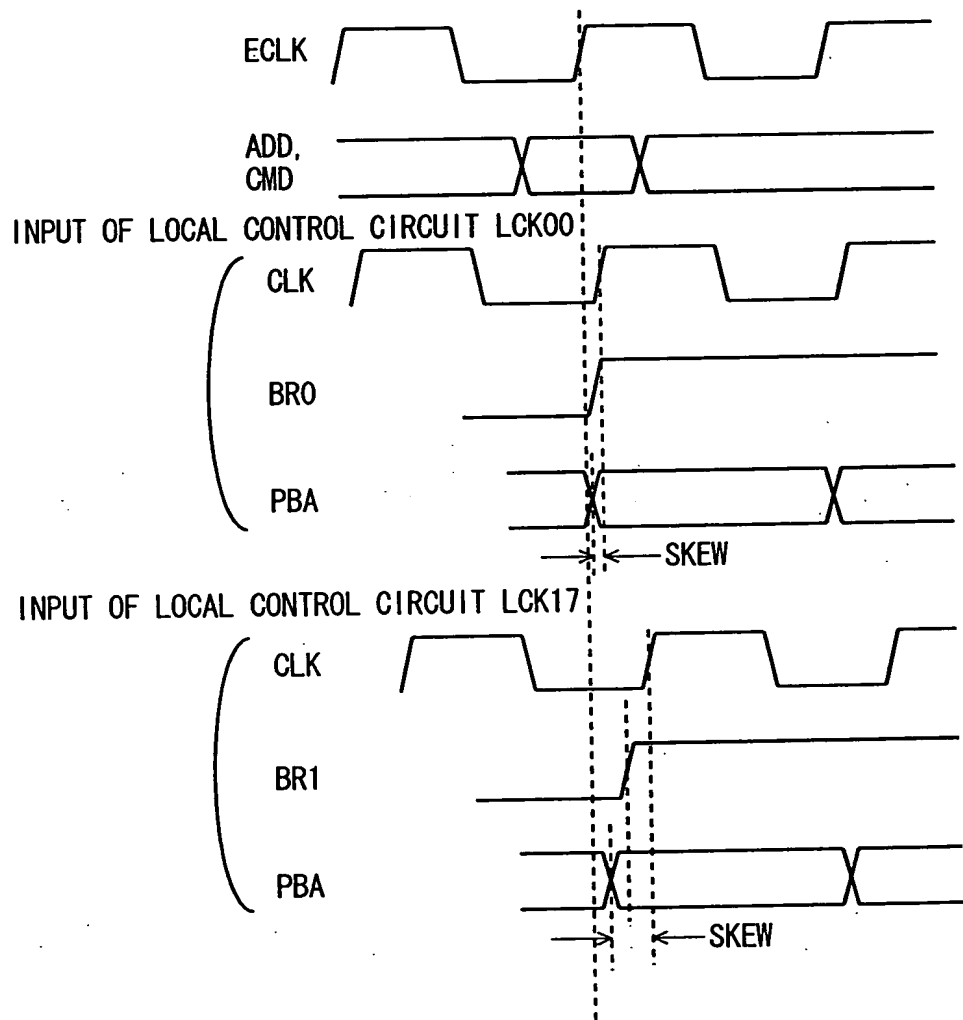


FIG.86 PRIOR ART

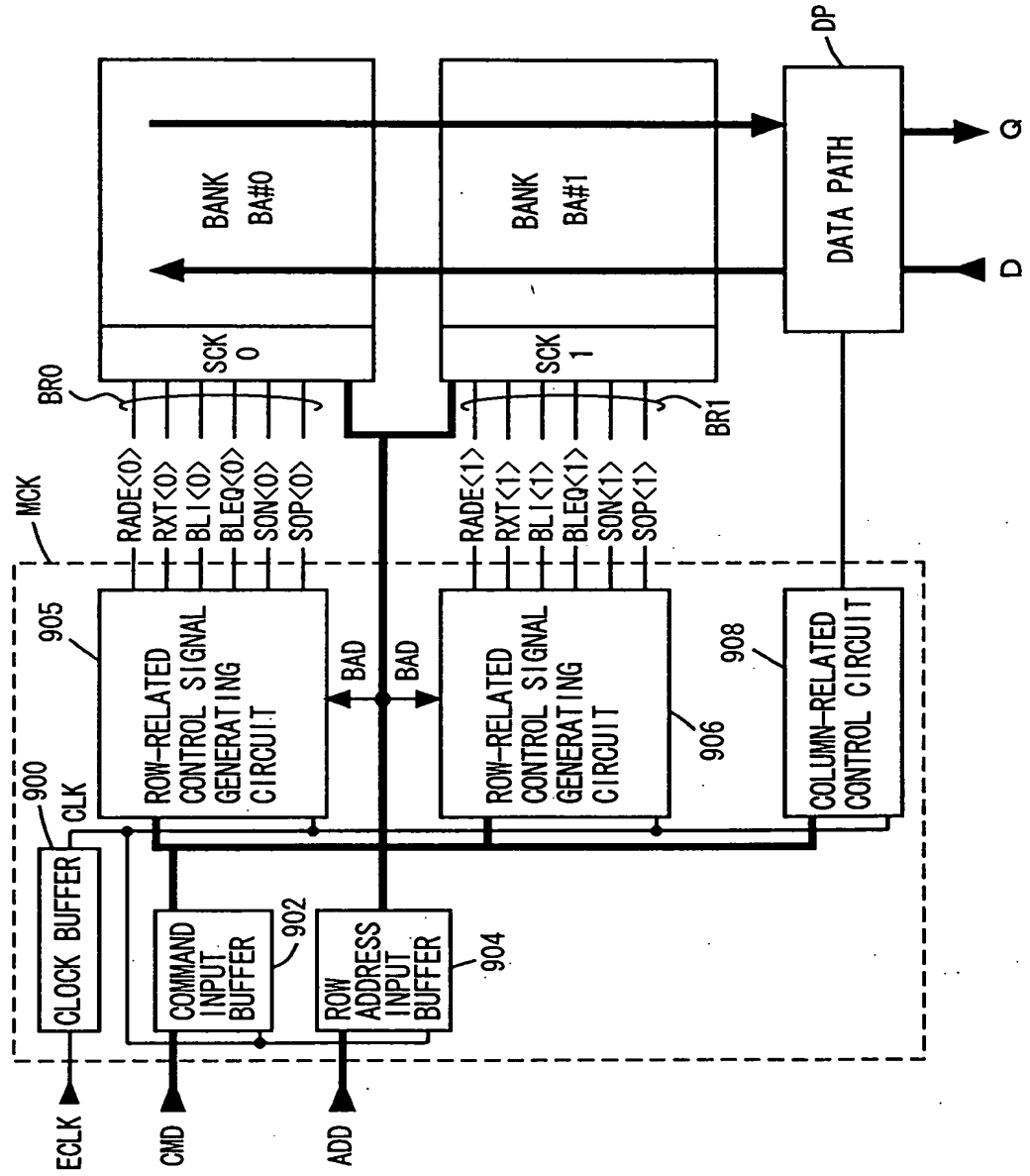


FIG.87 PRIOR ART

